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Applications Note

Product Name: 82C621A PCI IDE Controller

Title: Interrupt Handling and Pull-Up Requirement in Old Mode and New Mode

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Interrupt Handling

In the 82C621A, there are two mechanisms to translate the disk interrupts from the hard drives to the PCI bus. They can be selected through the New Mode and Old Mode strap options on pin 79. Level/edge interrupt strap option selected with Pin 45 and fixed/relocatable addresses selected with Pin 80 (please refer to the following table). Different strappings are recommended for on-board or peripheral card applications.

Pin 79	**Old Mode, pull up**				**New Mode, pull down**	
Interrupt Type	**Edge**		**Level**		**Edge**	**Level**
Pin #	**45**	**80**	**45**	**80**	**45***	**45***
Legacy (Fixed Address)	Pull Down	Pull Down	Pull Up	Pull Down	Pull Down	Not Available
Native (Relocatable Address)	Pull Down	Pull Up	Pull Up	Pull Up	Not Available	Pull Up

* Pin 80 should be at any valid logic level

When the 82C621A is built into a motherboard design, New Mode and Native Mode strapping is recommended. Under this strapping condition, pin 84 is connected to INTA# on the PCI bus. The 82C621A will translate the hard disk interrupt to a PCI type level trigger interrupt. For the New Mode and Legacy Mode strapping, the 82C621A will directly pass the edge trigger disk interrupt to the output pin IRQ14 (pin 47). Under this strapping condition, pin 47 needs to be connected directly to IRQ14 of the ISA bus interrupt controller or to INTA# of the PCI bus controller which can handle edge trigger interrupt input, such as the OPTi 82C822.

When the 82C621A is built into a peripheral card design, Old Mode and level trigger strapping is recommended for PCI compliance. The 82C621A will generate level trigger interrupts INTA# signal (pin 84) to the PCI bus in both Legacy or Native mode.

In both applications, hard drive disk interrupts need to be routed through the 82C621A. It should not bypass the chip and directly connect to the ISA interrupt controller. Please refer to the following table for the interrupt handling of the 82C621A under different strap options:

Actual mode of operation	**Interrupt level Strap**	**Pin (old mode)**			**Pin (new mode)**		
		84	**85**	**47**	**84**	**85**	**47**
Legacy	Edge	14	15	14	Tri-stated	15	14
Legacy	Level	14#	15#	14	Tri-stated	15	14
Native	Edge	14	15	Tri-stated	INTA#	Tri-stated	Tri-stated
Native	Level	14#	15#	Tri-stated	INTA#	Tri-stated	Tri-stated

Pull Up Requirement on the Disk Data Bus DD[15:0]

There is a 4.7K pull up requirement on the disk data bus DD[15:0] when the 82C621A is operating in the Old Mode. The 82C621A drives DD[15:0] only during disk write cycles. DD[15:0] are driven by the CMOS I/O buffer, therefore, floating the bus may draw large amounts of current and induce noise and heating problems which can damage the chip in the long run.

The pull-up requirement is not needed in the New Mode because DD[15:0] is driven by the 82C621A at all the times, except during disk read cycles.