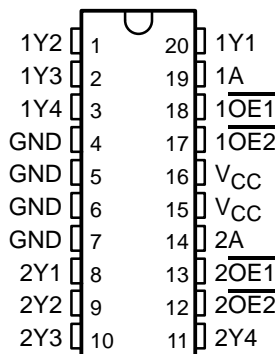


CDC209, CDC209-7 DUAL 1-LINE TO 4-LINE CLOCK DRIVERS WITH 3-STATE OUTPUTS

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- CDC209 Replaces 74AC11208
- CDC209-7 Replaces 74AC11208-7
- Low-Skew Propagation Delay Specifications for Clock-Driver Applications
- CMOS-Compatible Inputs and Outputs
- Flow-Through Architecture Optimizes PCB Layout
- Characterized for Operation at 5-V and 3.3-V V_{CC}
- Center-Pin V_{CC} and GND Pin Configurations Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- μ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic Small-Outline Package (DW) and Standard Plastic 300-mil DIPs (N)

DW OR N PACKAGE
(TOP VIEW)



description

The CDC209/209-7 contains dual clock-driver circuits that fanout one input signal to four outputs with minimum skew for clock distribution (see Figure 2). The device also offers two output-enable ($\overline{OE1}$ and $\overline{OE2}$) inputs for each circuit that can force the outputs to be disabled to a high-impedance state or to a high- or low-logic level independent of the signal on the respective A input.

Skew parameters are specified for a reduced temperature and voltage range common to many applications.

The CDC209/209-7 is characterized for operation from -40°C to 85°C .

FUNCTION TABLES

INPUTS			OUTPUTS			
$\overline{1OE1}$	$\overline{1OE2}$	1A	1Y1	1Y2	1Y3	1Y4
L	L	L	L	L	L	L
L	L	H	H	H	H	H
L	H	X	L	L	L	L
H	L	X	H	H	H	H
H	H	X	Z	Z	Z	Z

INPUTS			OUTPUTS			
$\overline{2OE1}$	$\overline{2OE2}$	2A	2Y1	2Y2	2Y3	2Y4
L	L	L	L	L	L	L
L	L	H	H	H	H	H
L	H	X	L	L	L	L
H	L	X	H	H	H	H
H	H	X	Z	Z	Z	Z



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**TEXAS
INSTRUMENTS**

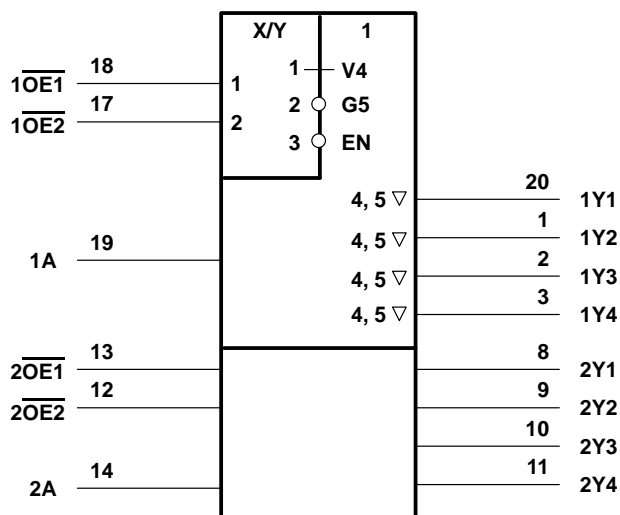
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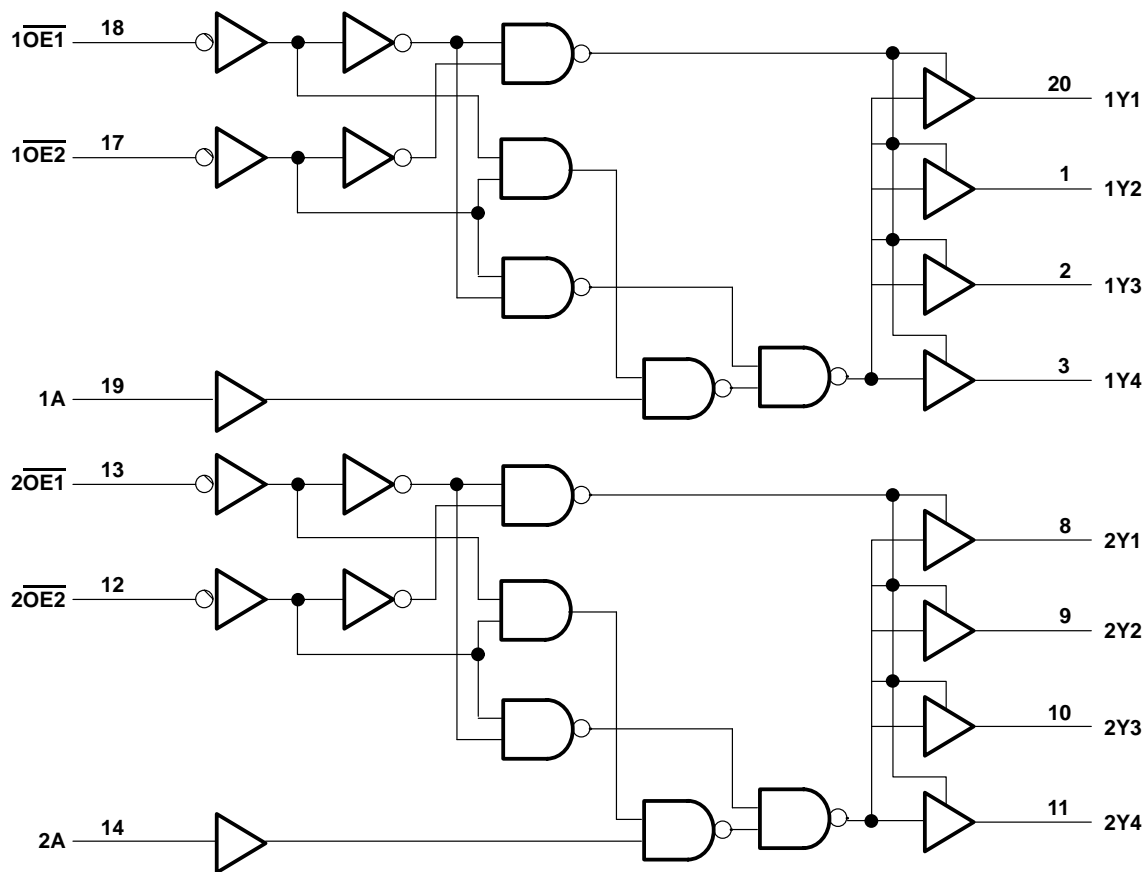
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND	±200 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2): DW package	1.6 W
N package	1.3 W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	5	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 3$ V	2.1		V
		$V_{CC} = 4.5$ V	3.15		
		$V_{CC} = 5.5$ V	3.85		
V_{IL}	Low-level input voltage	$V_{CC} = 3$ V		0.9	V
		$V_{CC} = 4.5$ V		1.35	
		$V_{CC} = 5.5$ V		1.65	
V_I	Input voltage	0		V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 3$ V		–4	mA
		$V_{CC} = 4.5$ V		–24	
		$V_{CC} = 5.5$ V		–24	
I_{OL}	Low-level output current	$V_{CC} = 3$ V		12	mA
		$V_{CC} = 4.5$ V		24	
		$V_{CC} = 5.5$ V		24	
$\Delta t / \Delta v$	Input transition rise or fall rate	0		10	ns/V
f_{clock}	Input clock frequency			60	MHz
T_A	Operating free-air temperature	–40		85	°C



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			CDC209		CDC209-7		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 µA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I _{OH} = -4 mA	3 V	2.58			2.48		2.48		
		4.5 V	3.94			3.8		3.8		
	I _{OH} = -24 mA	5.5 V	4.94			4.8		4.8		
		5.5 V				3.85		3.85		
V _{OL}	I _{OL} = 50 µA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I _{OL} = 12 mA	3 V			0.36		0.44		0.44	
		4.5 V			0.36		0.44		0.44	
	I _{OL} = 24 mA	5.5 V			0.36		0.44		0.44	
		5.5 V					1.65		1.65	
I _I	V _I = V _{CC} or GND	5.5 V			±0.1		±1		±1	µA
I _{OZ}	V _O = V _{CC} or GND	5.5 V			±0.5		±5		±5	µA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			8		80		80	µA
C _i	V _I = V _{CC} or GND	5 V		4						pF
C _o	V _O = V _{CC} or GND	5 V		10						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T _A = 25°C			CDC209		CDC209-7		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	1A and 2A	Any Y	4.8	11.1	13.1	4.8	14.6	4.8	14.6	ns
t _{PHL}			5.1	12.2	14.3	5.1	15.6	5.1	15.6	
t _{PLH}	1OE1, 1OE2, and 2OE1, 2OE2	Any Y	5.2	11.9	14.2	5.2	15.8	5.2	15.8	ns
t _{PHL}			7.8	13.3	15.7	7.8	17.4	7.8	17.4	
t _{PZH}	1OE2 or 2OE2	Any Y	5.1	11.8	14.2	5.1	15.7	5.1	15.7	ns
t _{PZL}	1OE1 or 2OE1		6.8	16.3	19.5	6.8	22.8	6.8	22.8	
t _{PHZ}	1OE2 or 2OE2	Any Y	3.4	6.9	8.6	3.4	9.2	3.4	9.2	ns
t _{PLZ}	1OE1 or 2OE1		4.1	7.5	9.4	4.1	10.2	4.1	10.2	

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DUAL 1-LINE TO 4-LINE CLOCK DRIVERS

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switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			CDC209		CDC209-7		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	1A and 2A	Any Y	4.2	5.5	9	4.2	9.9	4.2	9.9	ns
t_{PHL}			4.2	7	9.3	4.2	10.1	4.2	10.1	
t_{PLH}	$\overline{1OE1}$, $\overline{1OE2}$, and $\overline{2OE1}$, $\overline{2OE2}$	Any Y	4.6	7.3	9.6	4.6	10.7	4.6	10.7	ns
t_{PHL}			4.8	7.7	10.2	4.8	11	4.8	11	
t_{PZH}	$\overline{1OE2}$ or $\overline{2OE2}$	Any Y	4.3	7.2	9.4	4.3	10.4	4.3	10.4	ns
t_{PZL}	$\overline{1OE1}$ or $\overline{2OE1}$		5.3	9	12.2	5.3	13.5	5.3	13.5	
t_{PHZ}	$\overline{1OE2}$ or $\overline{2OE2}$	Any Y	3	5.4	7.5	3	8	3	8	ns
t_{PLZ}	$\overline{1OE1}$ or $\overline{2OE1}$		3.7	5.7	7.5	3.7	8.2	3.7	8.2	

switching characteristics, $V_{CC} = 5\text{ V} \pm 0.25\text{ V}$, $T_A = 25^\circ\text{C}$ to 70°C (see Note 3 and Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CDC209		CDC209-7		UNIT
			MIN	MAX	MIN	MAX	
t_{PLH}	1A and 2A	Any Y	6	8.5	6	8.5	ns
t_{PHL}			6	8.5	6	8.5	
$t_{sk(o)}$	1A and 2A	Any Y		1		0.7	ns

NOTE 3: All specifications are valid only for all outputs switching simultaneously and in phase.

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance per bank	C _L = 50 pF, f = 1 MHz	95	pF
	Outputs disabled		10	

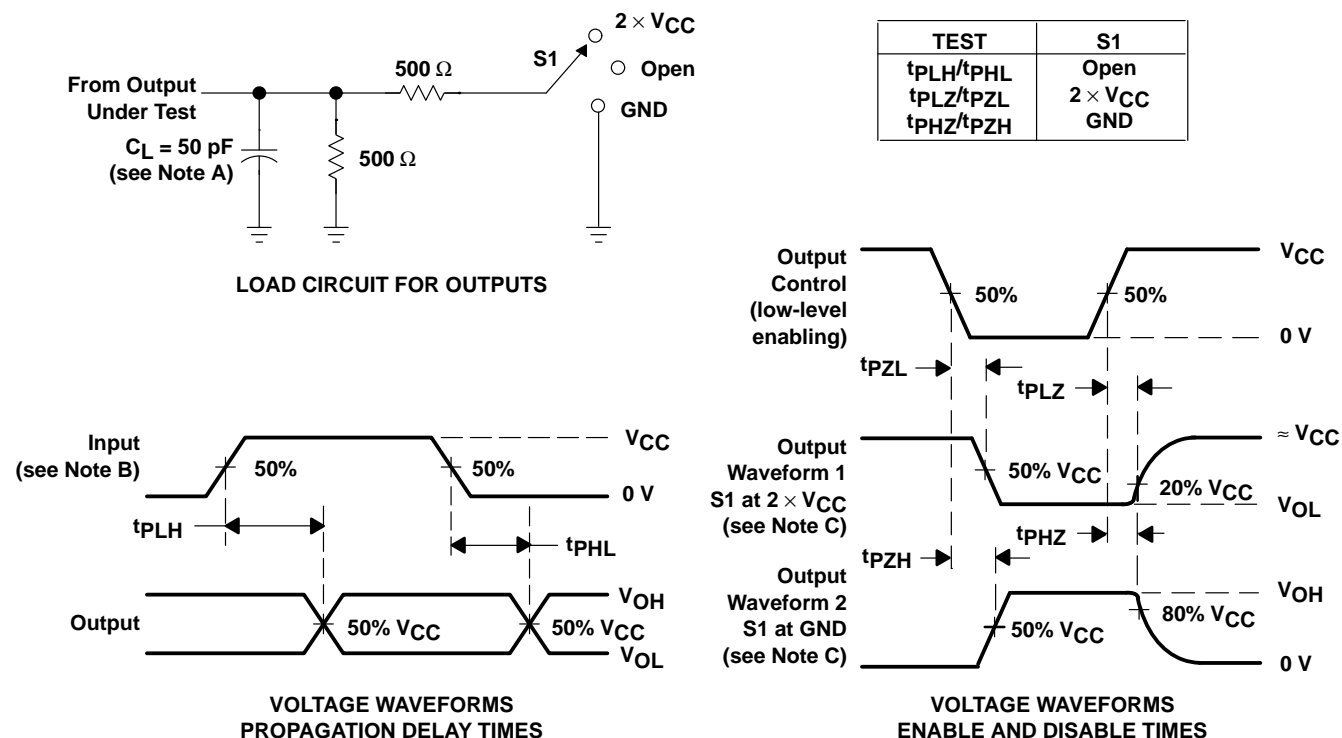
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WITH 3-STATE OUTPUTS

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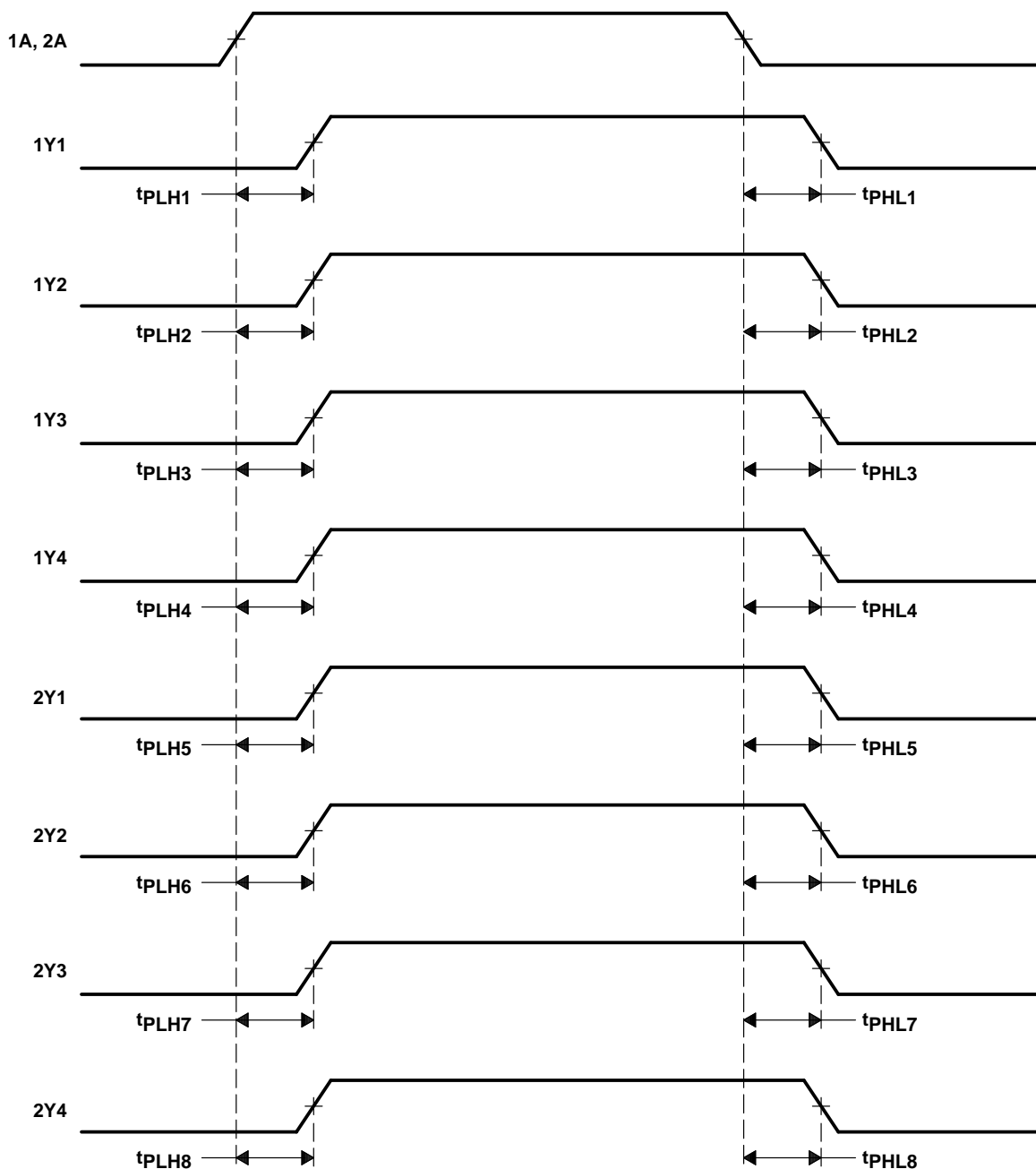
PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
- B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 3 \text{ ns}$, $t_f \leq 3 \text{ ns}$. For testing pulse duration: $t_r = t_f = 1 \text{ to } 3 \text{ ns}$. Pulse polarity can be either high-to-low-to-high or low-to-high-to-low.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTE A: Output skew, $t_{sk(o)}$, is calculated as the greater of:

- The difference between the fastest and slowest of t_{PLHn} ($n = 1, 2, \dots, 8$)
- The difference between the fastest and slowest of t_{PHLn} ($n = 1, 2, \dots, 8$)

Figure 2. Waveforms for Calculation of $t_{sk(o)}$

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