

# 54AC16244, 74AC16244 16-BIT BUFFERS/LINE DRIVERS WITH 3-STATE OUTPUTS

SCAS120A – MARCH 1990 – REVISED APRIL 1996

- Members of the Texas Instruments *Widebus*™ Family
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- Flow-Through Architecture Optimizes PCB Layout
- Distributed  $V_{CC}$  and GND Configuration Minimizes High-Speed Switching Noise
- *EPIC*™ (Enhanced-Performance Implanted CMOS) 1- $\mu$ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages Using 25-mil Center-to-Center Pin Spacings, and 380-mil Fine-Pitch Ceramic Flat (WD) Packages Using 25-mil Center-to-Center Pin Spacings

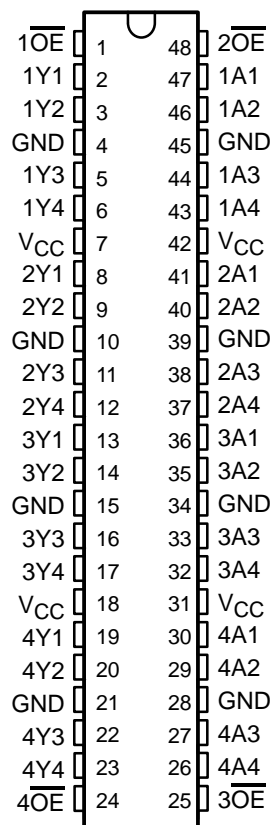
## description

The 'AC16244 are 16-bit buffers/line drivers designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. They can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. These devices provide true outputs and symmetrical active-low output-enable ( $\overline{OE}$ ) inputs. When  $\overline{OE}$  is low, the device passes noninverted data from the A inputs to the Y outputs. When  $\overline{OE}$  is high, the outputs are in the high-impedance state.

The 74AC16244 is packaged in the TI's shrink small-outline package, which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The 54AC16244 is characterized for operation over the full military temperature range of –55°C to 125°C. The 74AC16244 is characterized for operation from –40°C to 85°C.

54AC16244 . . . WD PACKAGE  
74AC16244 . . . DGG OR DL PACKAGE  
(TOP VIEW)



FUNCTION TABLE  
(each driver)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z



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**TEXAS  
INSTRUMENTS**

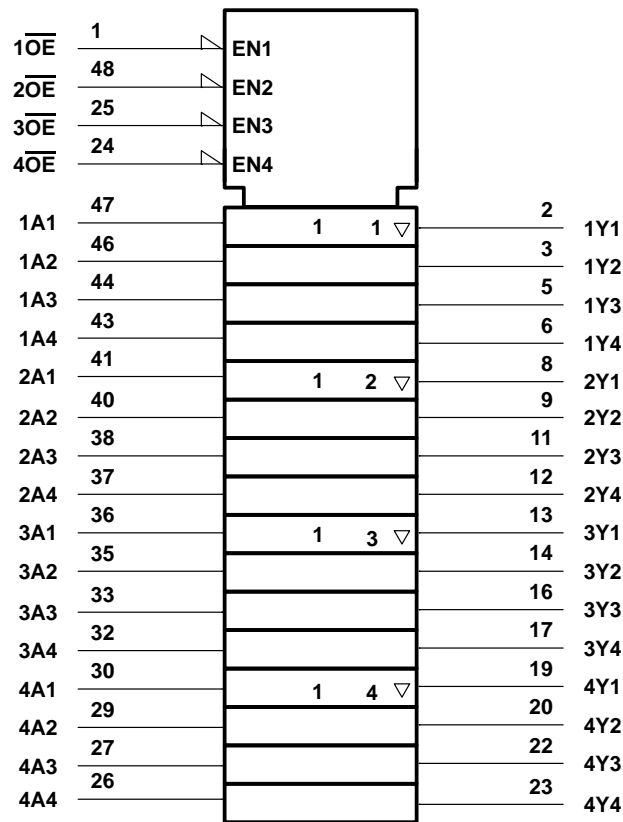
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logic symbol†

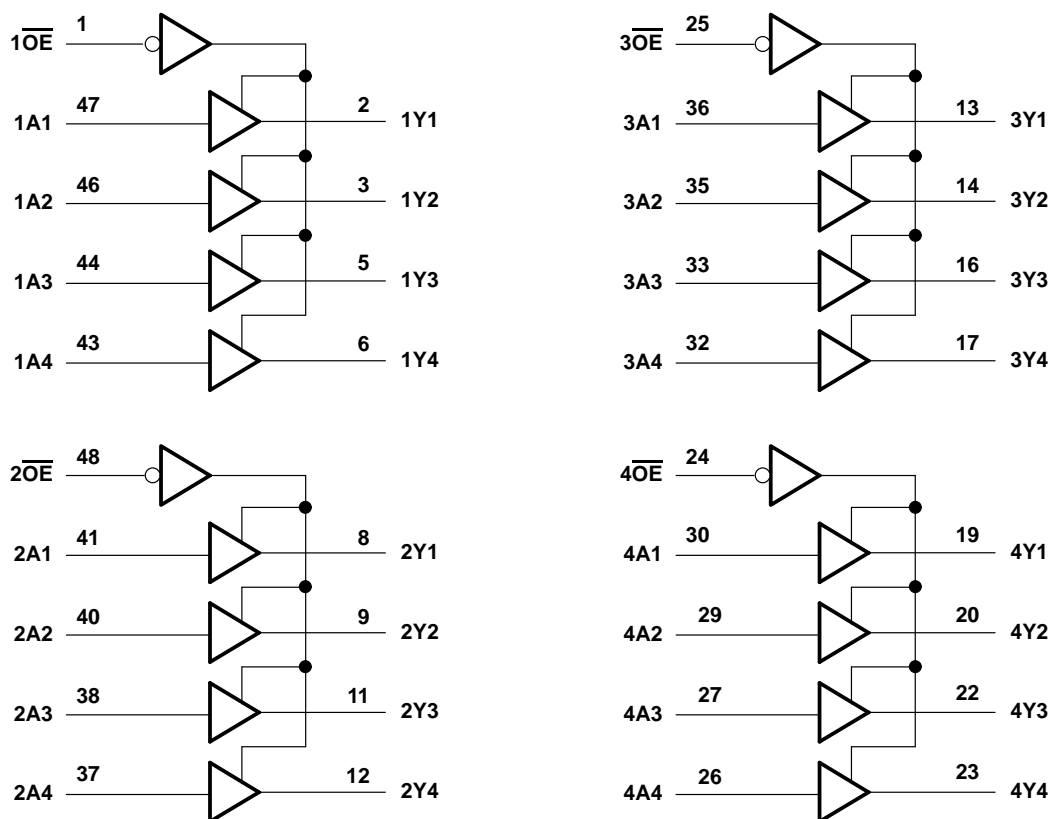


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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**logic diagram (positive logic)**



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>**

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, $V_O$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ )	±20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±50 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±50 mA
Continuous current through $V_{CC}$ or GND	±400 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2):	
DGG package	0.85 W
DL package	1.2 W
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

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## 16-BIT BUFFERS/LINE DRIVERS

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#### recommended operating conditions (see Note 3)

			54AC16244			74AC16244			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage (see Note 4)		3	5	5.5	3	5	5.5	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 3 V	2.1			2.1			V
		V <sub>CC</sub> = 4.5 V	3.15			3.15			
		V <sub>CC</sub> = 5.5 V	3.85			3.85			
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 3 V	0.9			0.9			V
		V <sub>CC</sub> = 4.5 V	1.35			1.35			
		V <sub>CC</sub> = 5.5 V	1.65			1.65			
V <sub>I</sub>	Input voltage		0	V <sub>CC</sub>		0	V <sub>CC</sub>		V
V <sub>O</sub>	Output voltage		0	V <sub>CC</sub>		0	V <sub>CC</sub>		V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 3 V	−4			−4			mA
		V <sub>CC</sub> = 4.5 V	−24			−24			
		V <sub>CC</sub> = 5.5 V	−24			−24			
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 3 V	12			12			mA
		V <sub>CC</sub> = 4.5 V	24			24			
		V <sub>CC</sub> = 5.5 V	24			24			
Δt/Δv	Input transition rise or fall rate		0	10		0	10		ns/V
T <sub>A</sub>	Operating free-air temperature		−55	125		−40	85		°C

NOTES: 3. Unused inputs should be tied to V<sub>CC</sub> through a pullup resistor of approximately 5 kΩ or greater to prevent them from floating.

4. All V<sub>CC</sub> and GND pins must be connected to the proper voltage supply.

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			54AC16244		74AC16244		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I <sub>OH</sub> = -4 mA	3 V	2.58			2.48		2.48		
		4.5 V	3.94			3.8		3.8		
		5.5 V	4.94			4.8		4.8		
	I <sub>OH</sub> = -75 mA†	5.5 V				3.85		3.85		
V <sub>OL</sub>	I <sub>OL</sub> = -50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I <sub>OL</sub> = 12 mA	3 V			0.36		0.44		0.44	
		4.5 V			0.36		0.44		0.44	
		5.5 V			0.36		0.44		0.44	
	I <sub>OL</sub> = 75 mA†	5.5 V				1.65		1.65		
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V			±0.1		±1		±1	μA
I <sub>OZ</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V			±0.5		±5		±5	μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			8		80		80	μA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		4.5						pF
C <sub>o</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		12						

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

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switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			54AC16244		74AC16244		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A	Y	2	7.1	9.4	2	10.8	2	10.8	ns
$t_{PHL}$			2.4	8.3	10.7	2.4	11.8	2.4	11.8	
$t_{PZH}$	$\overline{OE}$	Y	2.2	7.5	10	2.2	11.5	2.2	11.5	ns
$t_{PZL}$			2.9	10.4	13	2.9	14.6	2.9	14.6	
$t_{PHZ}$	$\overline{OE}$	Y	4.1	6.8	8.4	4.1	9.1	4.1	9.1	ns
$t_{PLZ}$			3.7	6.5	8.1	3.7	8.8	3.7	8.8	

switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			54AC16244		74AC16244		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A	Y	1.6	4.6	6.3	1.6	7.1	1.6	7.1	ns
$t_{PHL}$			2	5.3	7	2	7.9	2	7.9	
$t_{PZH}$	$\overline{OE}$	Y	1.7	4.8	6.7	1.7	7.5	1.7	7.5	ns
$t_{PZL}$			2.2	6.1	8.1	2.2	9	2.2	9	
$t_{PHZ}$	$\overline{OE}$	Y	4	6.4	7.8	4	8.4	4	8.4	ns
$t_{PLZ}$			3.5	5.5	7.2	3.5	7.6	3.5	7.6	

operating characteristics,  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER			TEST CONDITIONS		TYP	UNIT
$C_{pd}$	Power dissipation capacitance per latch	Outputs enabled	$C_L = 50 \text{ pF}$	$f = 1 \text{ MHz}$	43	pF
		Outputs disabled			7	

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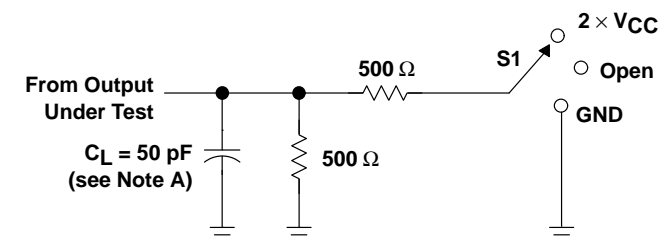
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## 16-BIT BUFFERS/LINE DRIVERS

### WITH 3-STATE OUTPUTS

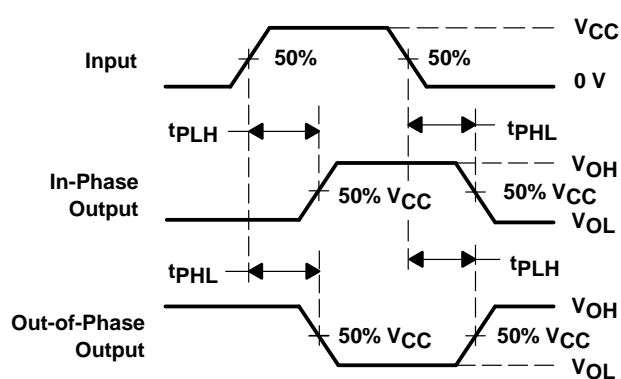
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#### PARAMETER MEASUREMENT INFORMATION

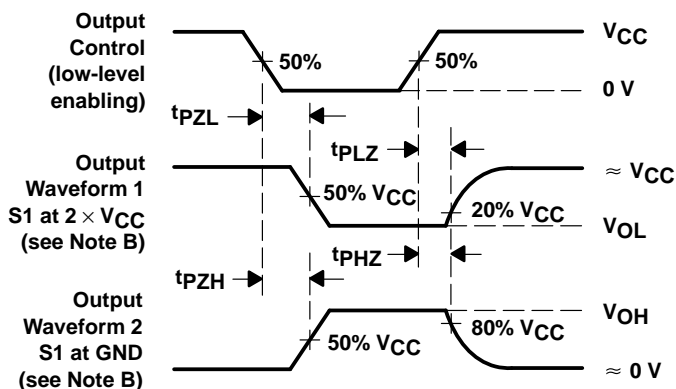


LOAD CIRCUIT

TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	2 $\times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = 3 \text{ ns}$ ,  $t_f = 3 \text{ ns}$ .
  - The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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