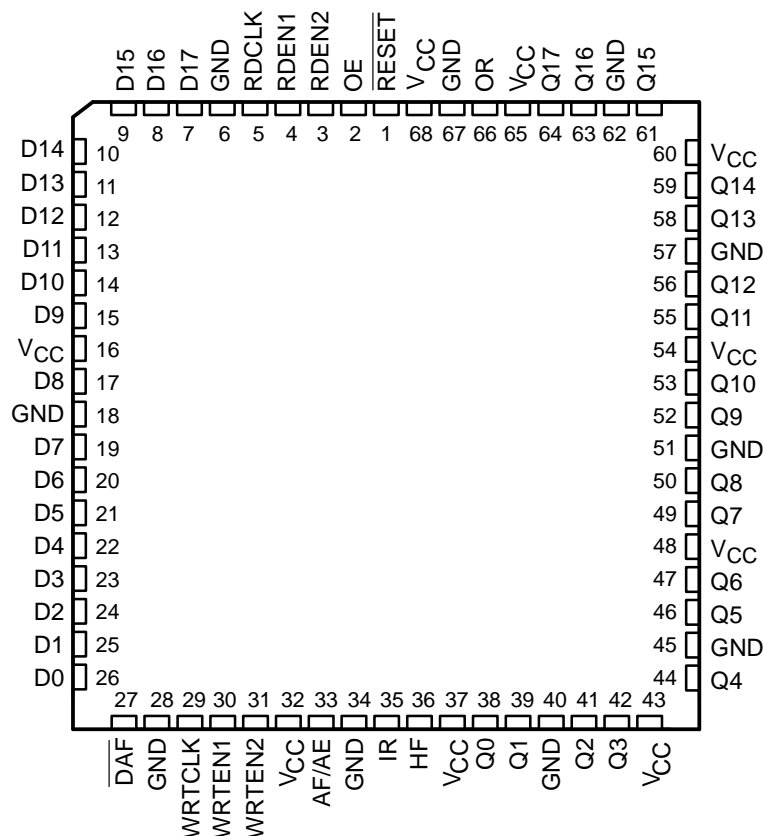


CLOCKED FIRST-IN, FIRST-OUT MEMORY

SCAS151C – JANUARY 1991 – REVISED FEBRUARY 1996

- Member of the Texas Instruments Widebus™ Family
- Independent Asynchronous Inputs and Outputs
- 1024 Words × 18 Bits
- Read and Write Operations Can Be Synchronized to Independent System Clocks
- Programmable Almost-Full/Almost-Empty Flag
- Pin-to-Pin Compatible With SN74ACT7881, SN74ACT7882, and SN74ACT7884
- Input-Ready, Output-Ready, and Half-Full Flags
- Cascadable in Word Width and/or Word Depth
- Fast Access Times of 15 ns With a 50-pF Load
- High-Output Drive for Direct Bus Interface
- Available in 68-Pin PLCC (FN) and Space-Saving 80-Pin Thin Quad Flat (PN) Packages

FN PACKAGE
(TOP VIEW)

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments Incorporated.

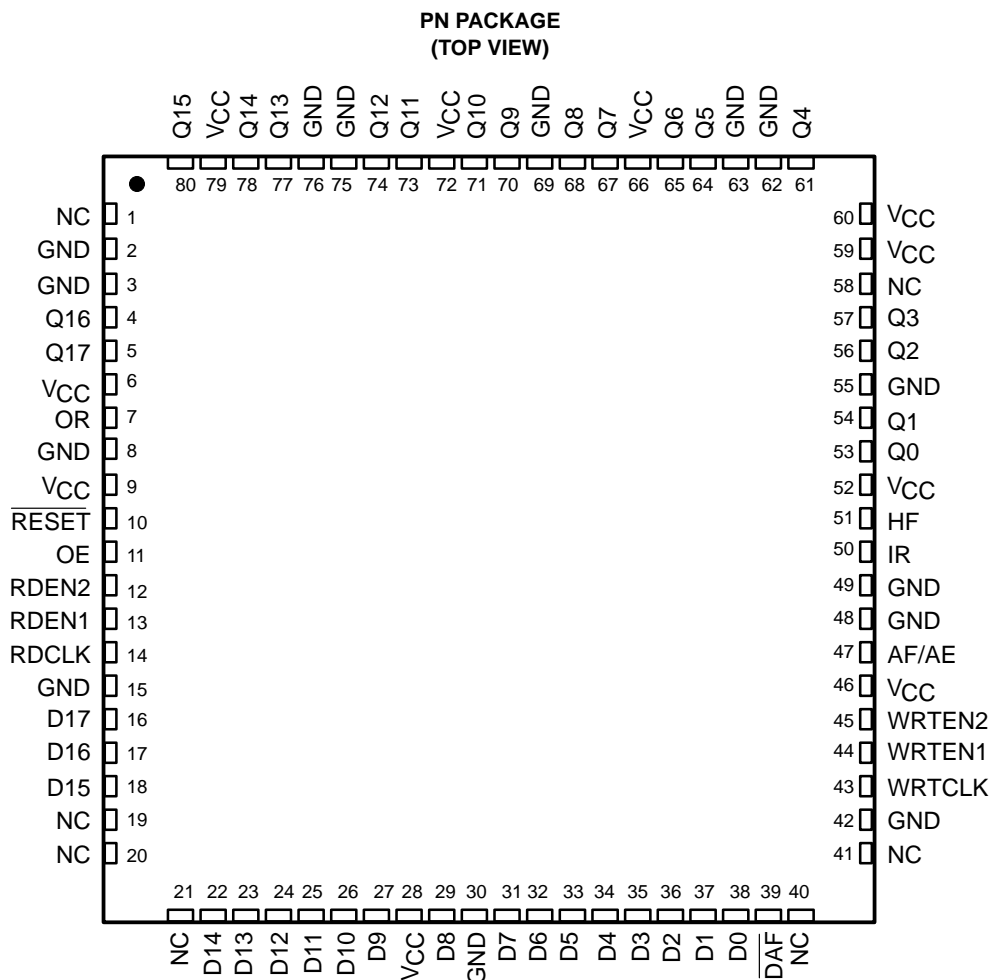
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1996, Texas Instruments Incorporated

SN74ACT7811
1024 × 18
CLOCKED FIRST-IN, FIRST-OUT MEMORY
 SCAS151C – JANUARY 1991 – REVISED FEBRUARY 1996



NC – No internal connection

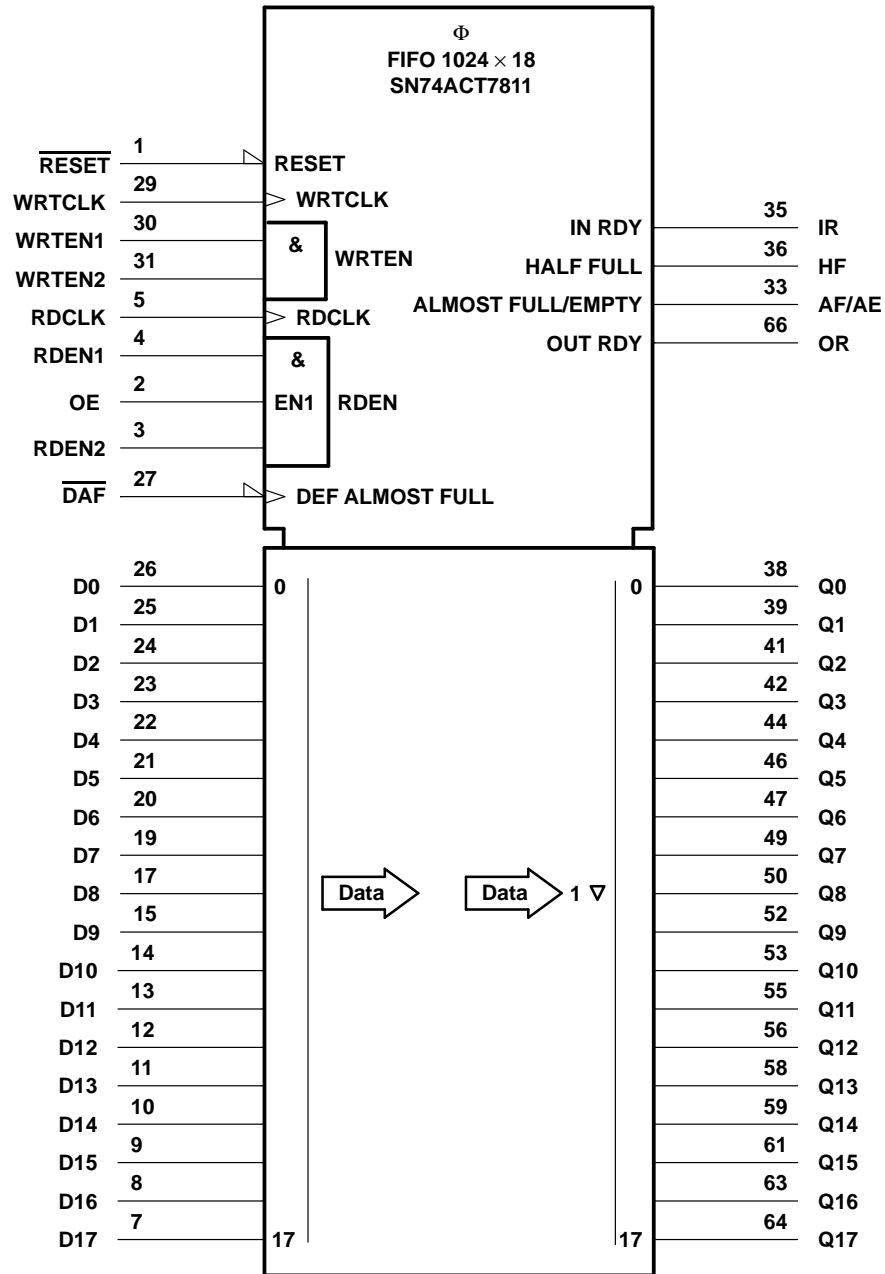
description

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The SN74ACT7811 is a 1024 × 18-bit FIFO for high speed and fast access times. It processes data at rates up to 40 MHz and access times of 15 ns in a bit-parallel format. Data outputs are noninverting with respect to the data inputs. Expansion is easily accomplished in both word width and word depth.

The SN74ACT7811 has normal input-bus-to-output-bus asynchronous operation. The special enable circuitry adds the ability to synchronize independent read and write (interrupts or requests) to their respective system clock.

The SN74ACT7811 is characterized for operation from 0°C to 70°C.

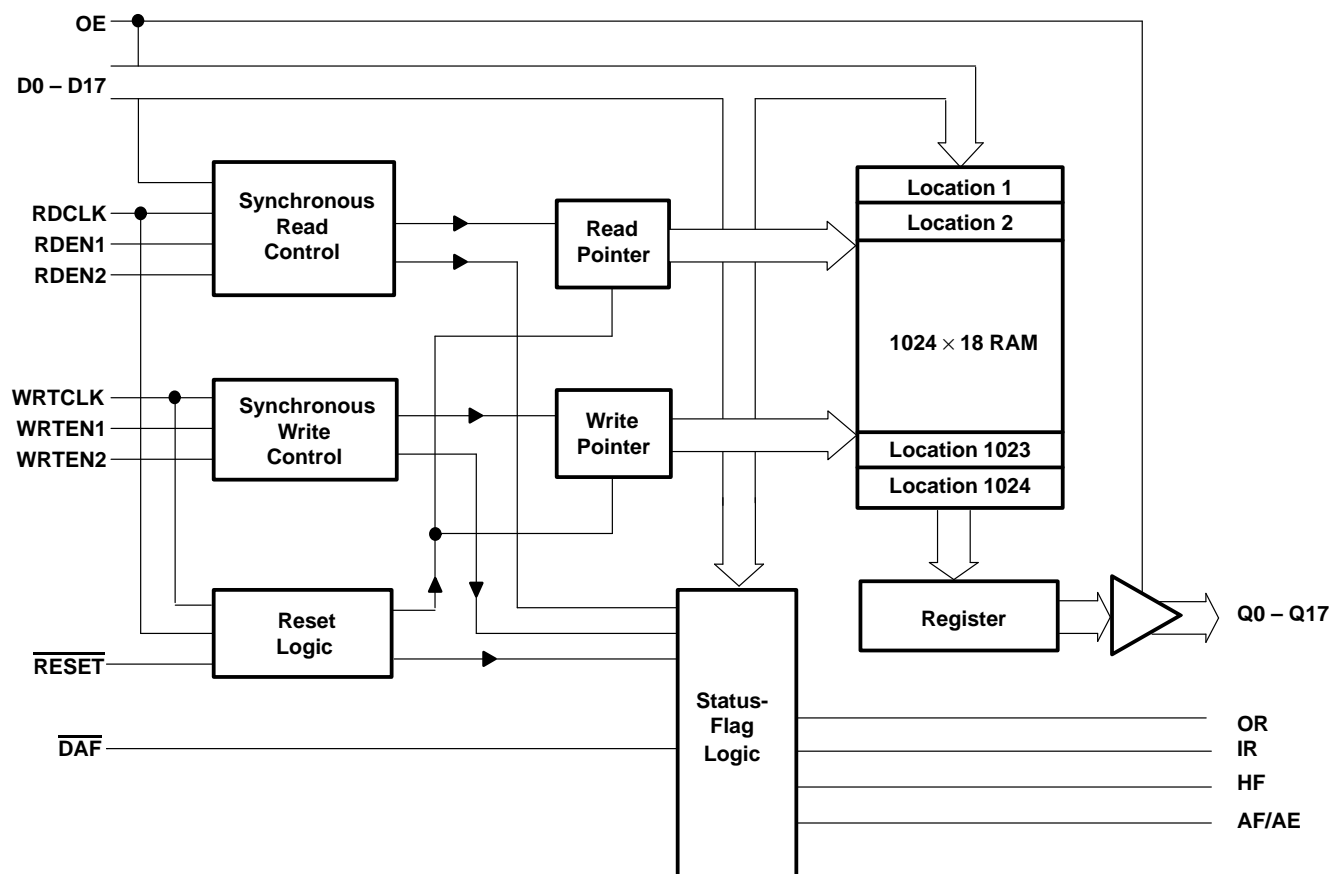
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the FN package.

SN74ACT7811
1024 × 18
CLOCKED FIRST-IN, FIRST-OUT MEMORY
 SCAS151C – JANUARY 1991 – REVISED FEBRUARY 1996

functional block diagram



Terminal Functions

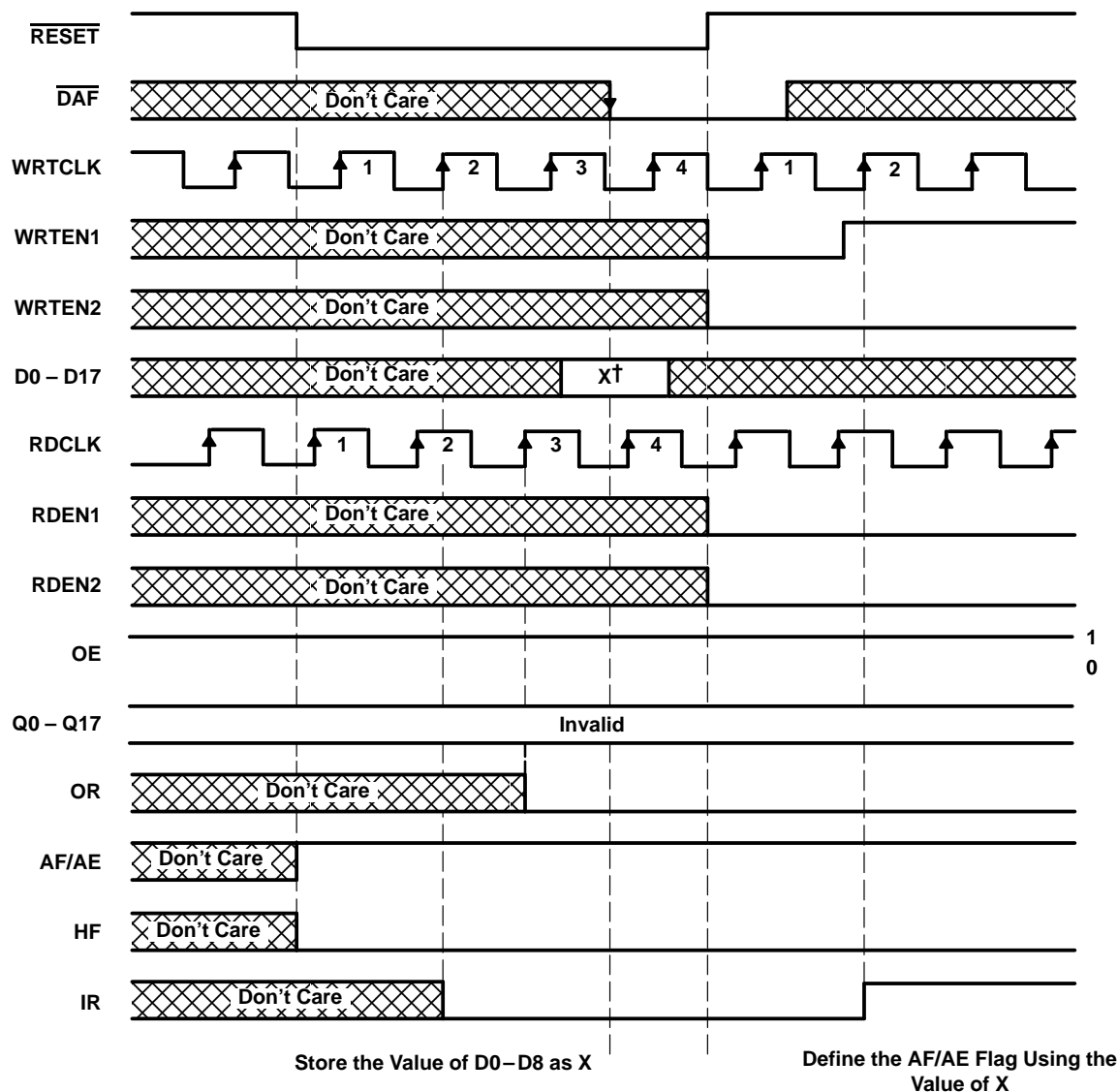
TERMINAL† NAME	NO.	I/O	DESCRIPTION
AF/AE	33	O	<p>Almost-full/almost-empty flag. The AF/AE boundary is defined by the almost-full/almost-empty offset value (X). This value can be programmed during reset or the default value of 256 can be used. AF/AE is high when the FIFO contains (X + 1) or less words or (1025 - X) or more words. AF/AE is low when the FIFO contains between (X + 2) and (1024 - X) words.</p> <p>Programming procedure for AF/AE – The almost-full/almost-empty flag is programmed during each reset cycle. The almost-full/almost-empty offset value (X) is either a user-defined value or the default of X = 256. Instructions to program AF/AE using both methods are as follows:</p> <p><u>User-defined X</u></p> <p>Step 1: Take $\overline{\text{DAF}}$ from high to low.</p> <p>Step 2: If $\overline{\text{RESET}}$ is not already low, take $\overline{\text{RESET}}$ low.</p> <p>Step 3: With $\overline{\text{DAF}}$ held low, take $\overline{\text{RESET}}$ high. This defines the AF/AE using X.</p> <p>Step 4: To retain the current offset for the next reset, keep $\overline{\text{DAF}}$ low.</p> <p><u>Default X</u></p> <p>To redefine AF/AE using the default value of X = 256, hold $\overline{\text{DAF}}$ high during the reset cycle.</p>
$\overline{\text{DAF}}$	27	I	Define almost full. The high-to-low transition of $\overline{\text{DAF}}$ stores the binary value of data inputs as the almost-full/almost-empty offset value (X). With $\overline{\text{DAF}}$ held low, a low pulse on $\overline{\text{RESET}}$ defines the AF/AE flag using X.
D0–D17	26–19, 17, 15–7	I	Data inputs for 18-bit-wide data to be stored in the memory. Data lines D0–D8 also carry the almost-full/almost-empty offset value (X) on a high-to-low transition of the $\overline{\text{DAF}}$.
HF	36	O	Half-full flag. HF is high when the FIFO contains 513 or more words and is low when it contains 512 or less words.
IR	35	O	Input-ready flag. IR is high when the FIFO is not full and low when the device is full. During reset, IR is driven low on the rising edge of the second WRTCLK pulse. IR is then driven high on the rising edge of the second WRTCLK pulse after $\overline{\text{RESET}}$ goes high. After the FIFO is filled and IR is driven low, IR is driven high on the second WRTCLK pulse after the first valid read.
OE	2	I	Output enable. The data-out (Q0–Q17) outputs are in the high-impedance state when OE is low. OE must be high before the rising edge of RDCLK to read a word from memory.
OR	66	O	Output-ready flag. OR is high when the FIFO is not empty and low when it is empty. During reset, OR is set low on the rising edge of the third RDCLK pulse. OR is set high on the rising edge of the third RDCLK pulse to occur after the first word is written into the FIFO. OR is set low on the rising edge of the first RDCLK pulse after the last word is read.
Q0–Q17	38–39, 41–42, 44, 46–47, 49–50, 52–53, 55–56, 58–59, 61, 63–64	O	Data outputs. The first data word to be loaded into the FIFO is moved to Q0–Q17 on the rising edge of the third RDCLK pulse to occur after the first valid write. The RDEN1 and RDEN2 inputs do not affect this operation. Following data is unloaded on the rising edge of RDCLK when RDEN1, RDEN2, OE, and the OR are high.
RDCLK	5	I	Read clock. Data is read out of memory on a low-to-high transition RDCLK if OR, OE, and RDEN1 and RDEN2 control inputs are high. RDCLK is a free-running clock and functions as the synchronizing clock for all data transfers out of the FIFO. OR is also driven synchronously with respect to RDCLK.
RDEN1, RDEN2	4 3	I	Read enable. RDEN1 and RDEN2 must be high before a rising edge on RDCLK to read a word out of memory. RDEN1 and RDEN2 are not used to read the first word stored in memory.
$\overline{\text{RESET}}$	1	I	A reset is accomplished by taking $\overline{\text{RESET}}$ low and generating a minimum of four RDCLK and WRTCLK cycles. This ensures that the internal read and write pointers are reset and OR, HF, and IR are low and AF/AE is high. The FIFO must be reset upon power up. With $\overline{\text{DAF}}$ at a low level, a low pulse on $\overline{\text{RESET}}$ defines the AF/AE status flag using the almost-full/almost-empty offset value (X), where X is the value previously stored. With $\overline{\text{DAF}}$ at a high level, a low-level pulse on $\overline{\text{RESET}}$ defines the AF/AE flag using the default value of X = 256.

† Terminals listed are for the FN package.

Terminal Functions (Continued)

TERMINAL† NAME	NO.	I/O	DESCRIPTION
WRTCLK	29	I	Write clock. Data is written into memory on a low-to-high transition of WRTCLK if IR, WRTE1, and WRTE2 are high. WRTCLK is a free-running clock and functions as the synchronizing clock for all data transfers into the FIFO. IR is also driven synchronously with respect to WRTCLK.
WRTE1, WRTE2	30 31	I	Write enables. WRTE1 and WRTE2 must be high before a rising edge on WRTCLK for a word to be written into memory. WRTE1 and WRTE2 do not affect the storage of the almost-full/almost-empty offset value (X).

† Terminals listed are for the FN package.



† X is the binary value of D0–D8 only.

Figure 1. Reset Cycle: Define AF/AE Using the Value of X

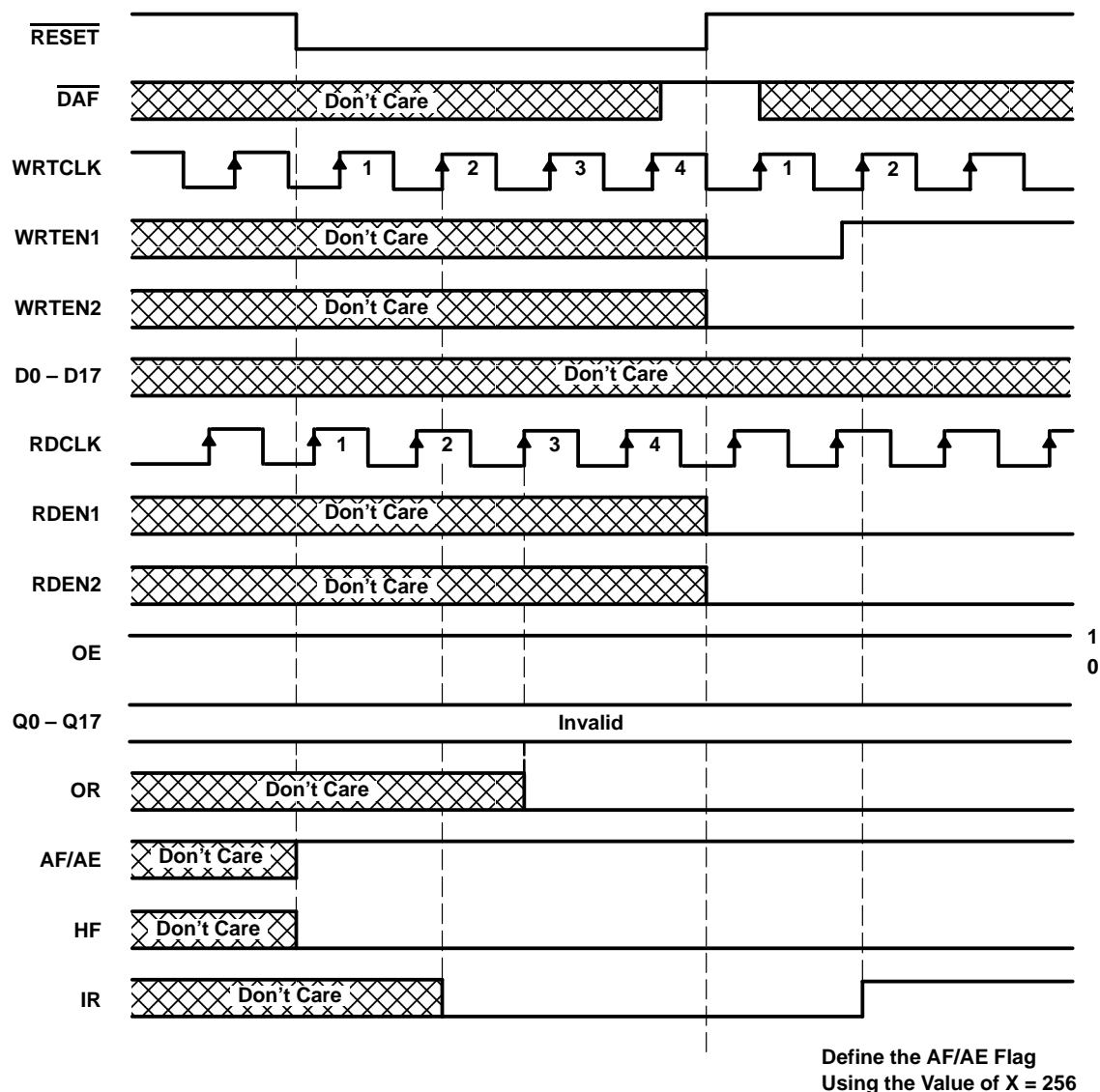


Figure 2. Reset Cycle: Define AF/AE Using the Default Value

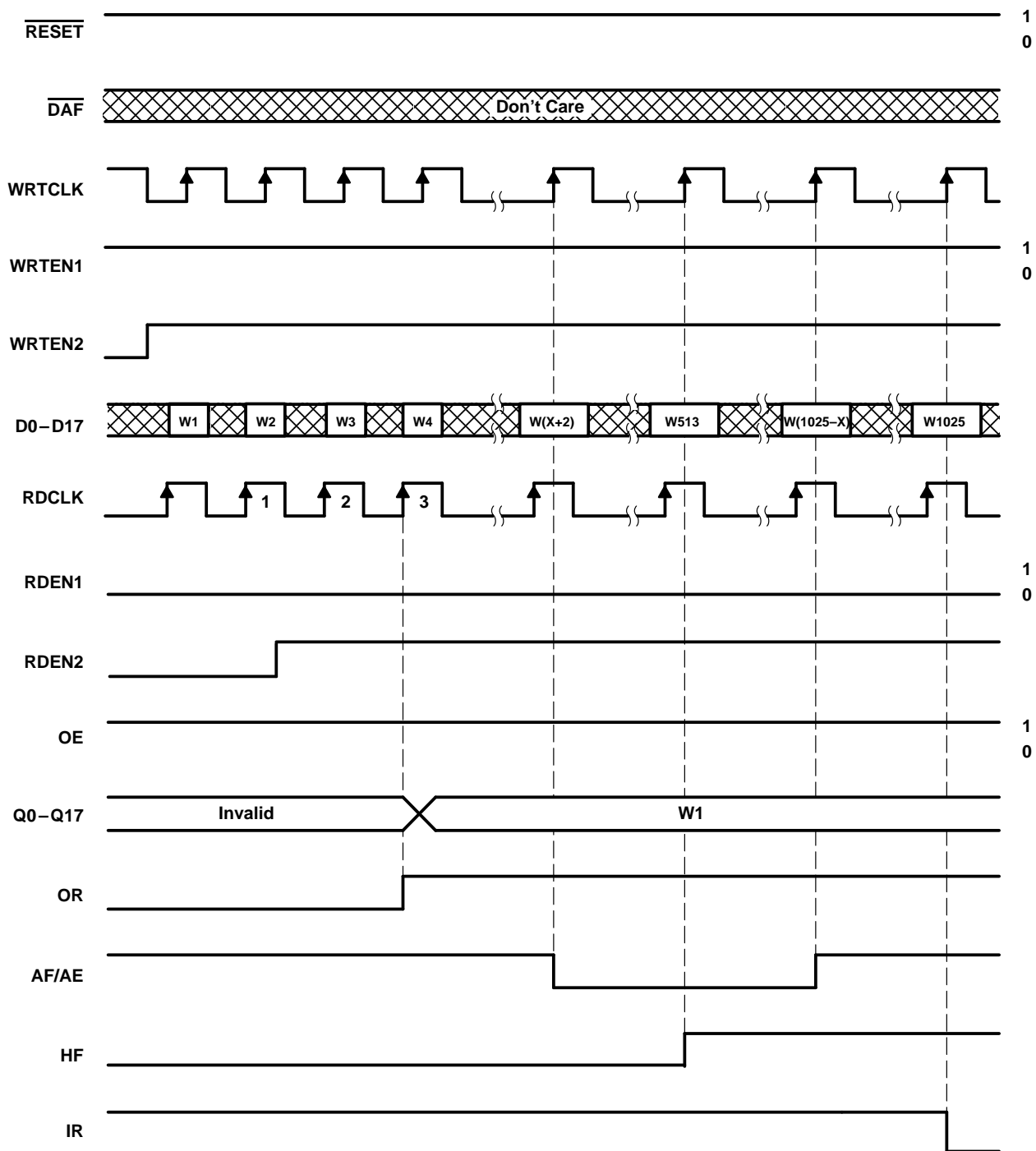


Figure 3. Write Cycle

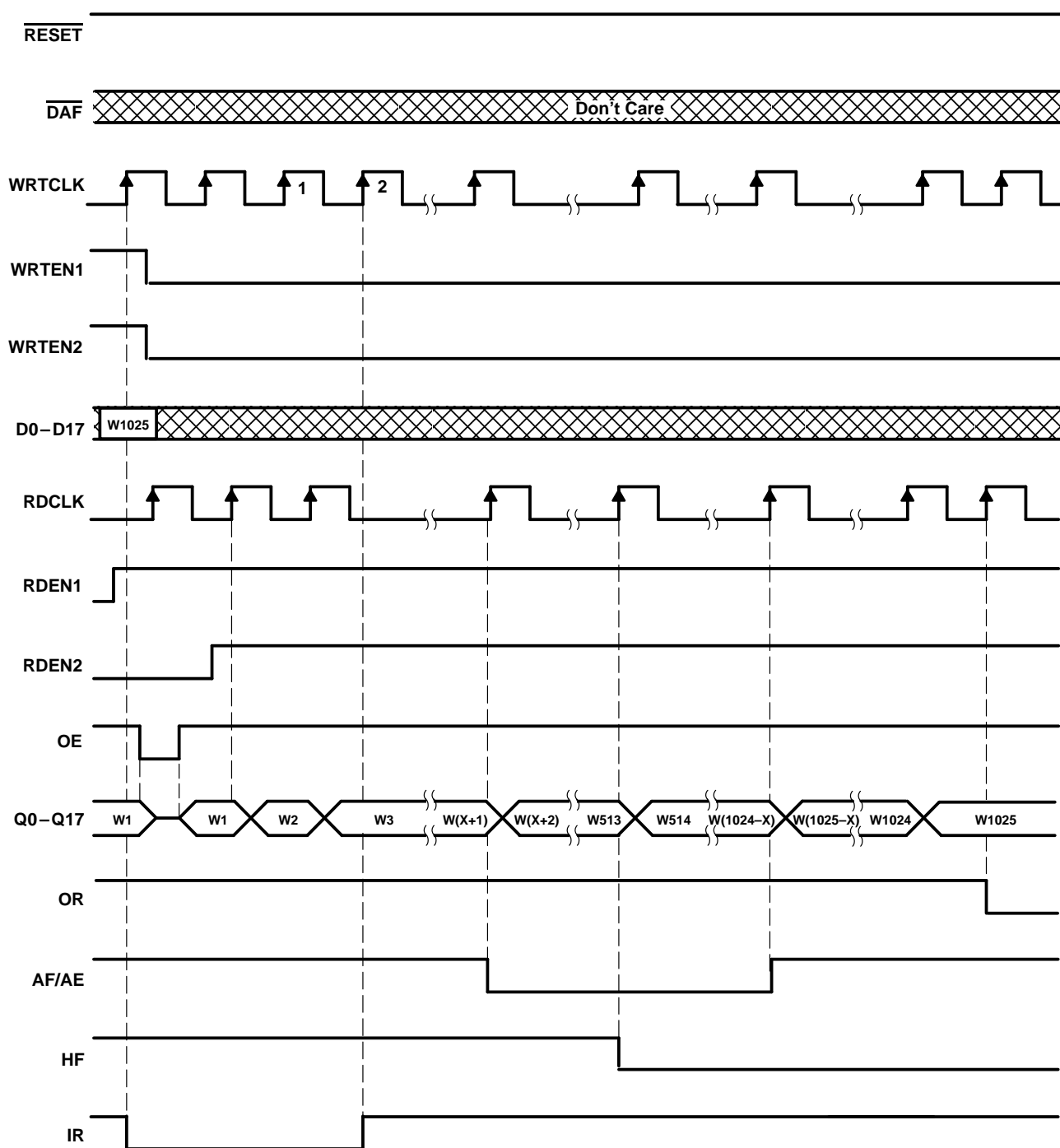


Figure 4. Read Cycle

SN74ACT7811
1024 × 18
CLOCKED FIRST-IN, FIRST-OUT MEMORY
 SCAS151C – JANUARY 1991 – REVISED FEBRUARY 1996

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage, V_I	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

	MIN	MAX	UNIT
V_{CC} Supply voltage	4.5	5.5	V
V_{IH} High-level input voltage	2		V
V_{IL} Low-level input voltage		0.8	V
I_{OH} High-level output current		–8	mA
I_{OL} Low-level output current		16	mA
T_A Operating free-air temperature	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
V_{OH}	$V_{CC} = 4.5$ V, $I_{OH} = -8$ mA	2.4			V
V_{OL}	$V_{CC} = 4.5$ V, $I_{OL} = 16$ mA			0.5	V
I_I	$V_{CC} = 5.5$ V, $V_I = V_{CC}$ or 0 V			±5	µA
I_{OZ}	$V_{CC} = 5.5$ V, $V_O = V_{CC}$ or 0 V			±5	µA
$I_{CC}§$	$V_I = V_{CC} - 0.2$ V or 0 V			400	µA
	One input at 3.4 V, Other inputs at V_{CC} or GND			1	mA
C_i	$V_I = 0$ V, $f = 1$ MHz		4		pF
C_o	$V_O = 0$ V, $f = 1$ MHz		8		pF

‡ All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

§ I_{CC} tested with outputs open

timing requirements (see Figures 1 through 8)

			'ACT7811-15		'ACT7811-18		'ACT7811-20		'ACT7811-25		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency		40		35		28.5		16.7		MHz
t _w	Pulse duration	D0–D17 high or low	10		12		14		20		ns
		WRTCLK high	7		8.5		10		17		
		WRTCLK low	10		11		14		23		
		RDCLK high	7		8.5		10		17		
		RDCLK low	10		11		14		23		
		DAF high	10		10		10		10		
		WR TEN1, WR TEN2 high or low	10		10		10		10		
		OE, RDEN1, RDEN2 high or low	10		10		10		10		
t _{su}	Setup time	D0–D17 before WRTCLK↑	5		5		5		5		ns
		WR TEN1, WR TEN2 high before WRTCLK↑	5		5		5		5		
		OE, RDEN1, RDEN2 high before RDCLK↑	5		5		5		5		
		Reset: RESET low before first WRTCLK and RDCLK↑	7		7		7		7		
		Define AF/AE: D0–D8 before DAF↓	5		5		5		5		
		Define AF/AE: DAF↓ before RESET↑	7		7		7		7		
		Define AF/AE (default): DAF high before RESET↑	5		5		5		5		
t _h	Hold time	D0–D17 after WRTCLK↑	1		1		1		1		ns
		WR TEN1, WR TEN2 high after WRTCLK↑	1		1		1		1		
		OE, RDEN1, RDEN2 high after RDCLK↑	1		1		1		1		
		Reset: RESET low after fourth WRTCLK and RDCLK↑	0		0		0		0		
		Define AF/AE: D0–D8 after DAF↓	1		1		1		1		
		Define AF/AE: DAF low after RESET↑	0		0		0		0		
		Define AF/AE (default): DAF high after RESET↑	1		1		1		1		

† To permit the clock pulse to be utilized for reset purposes

SN74ACT7811
1024 × 18
CLOCKED FIRST-IN, FIRST-OUT MEMORY
 SCAS151C – JANUARY 1991 – REVISED FEBRUARY 1996

switching characteristics over recommended operating free-air temperature range (see Figures 9 and 10)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 500 Ω, T _A = 0°C to 70°C								UNIT	
			'ACT7811-15			'ACT7811-18		'ACT7811-20		'ACT7811-25		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN		MAX
f _{max}	WRTCLK or RDCLK		40			35		28.5		16.7		MHz
t _{pd}	RDCLK↑	Any Q	4	12	15	4	18	4	20	4	25	ns
t _{pd} [†]			10.5									
t _{pd}	WRTCLK↑	IR	2			10		2		14		ns
t _{pd}	RDCLK↑	OR	2			10		2		14		ns
t _{pd}	WRTCLK↑	AF/AE	6			20		6		24		ns
	RDCLK↑		6			20		6		24		
t _{PLH}	WRTCLK↑	HF	6			19		6		23		ns
t _{PHL}	RDCLK↑		6			19		6		23		
t _{PLH}	RESET↓	AF/AE	3			19		3		23		ns
t _{PHL}		HF	4			21		4		25		
t _{en}	OE	Any Q	2			11		2		11		ns
t _{dis}			2			14		2		14		

† This parameter is measured with C_L = 30 pF (see Figure 5).

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance per 1K bits	C _L = 50 pF, f = 5 MHz	65	pF

TYPICAL CHARACTERISTICS

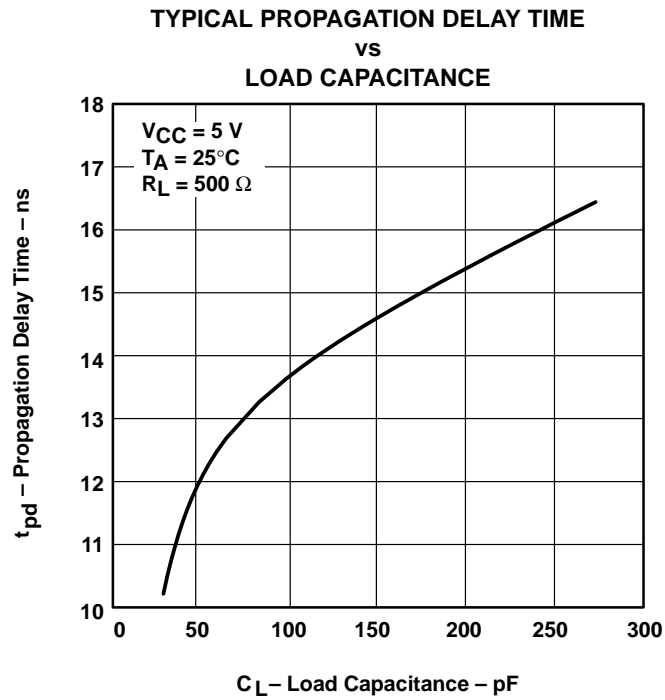


Figure 5

TYPICAL CHARACTERISTICS

TYPICAL POWER DISSIPATION CAPACITANCE
 vs
 SUPPLY VOLTAGE

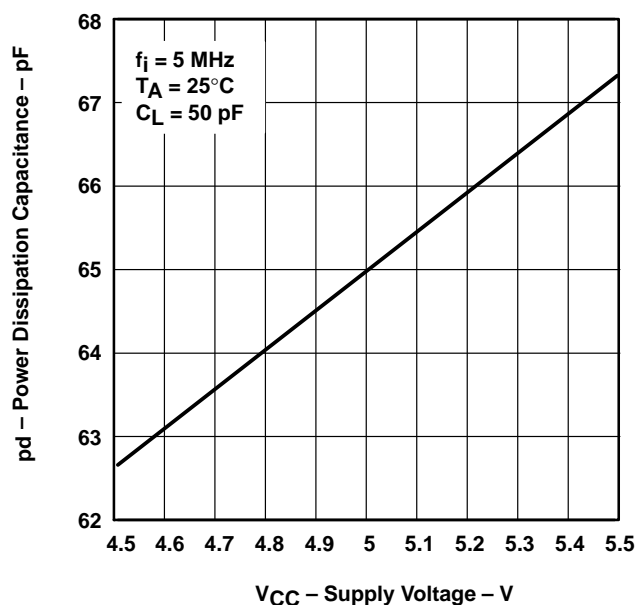


Figure 6

calculating power dissipation

The maximum power dissipation (P_T) of the SN74ACT7811 can be calculated by:

$$P_T = V_{CC} \times [I_{CC} + (N \times \Delta I_{CC} \times dc)] + \Sigma (C_{pd} \times V_{CC}^2 \times f_i) + \Sigma (C_L \times V_{CC}^2 \times f_o)$$

where:

- I_{CC} = power-down I_{CC} maximum
- N = number of inputs driven by a TTL device
- ΔI_{CC} = increase in supply current
- dc = duty cycle of inputs at a TTL high level of 3.4 V
- C_{pd} = power dissipation capacitance
- C_L = output capacitive load
- f_i = data input frequency
- f_o = data output frequency

APPLICATION INFORMATION

expanding the SN74ACT7811

The SN74ACT7811 is expandable in width and depth. Expanding in word depth offers special timing considerations:

After the first data word is loaded into the FIFO, the word is unloaded and the output-ready flag (OR) output goes high after $(N \times 3)$ read-clock (RDCLK) cycles, where N is the number of devices used in depth expansion.

After the FIFO is filled, the input-ready flag (IR) output goes low, the first word is unloaded, and the IR flag output is driven high after $(N \times 2)$ write-clock cycles, where N is the number of devices used in depth expansion.

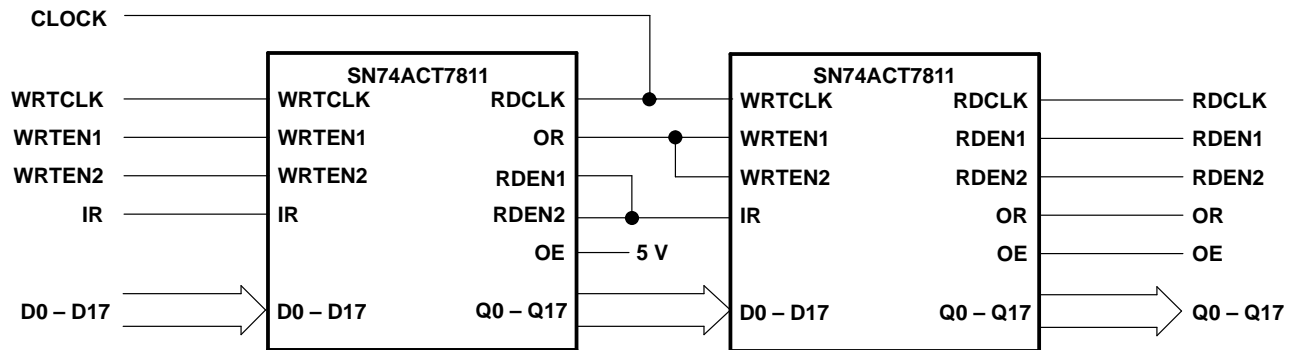


Figure 7. Word-Depth Expansion: 2048 Words × 18 Bits, N = 2

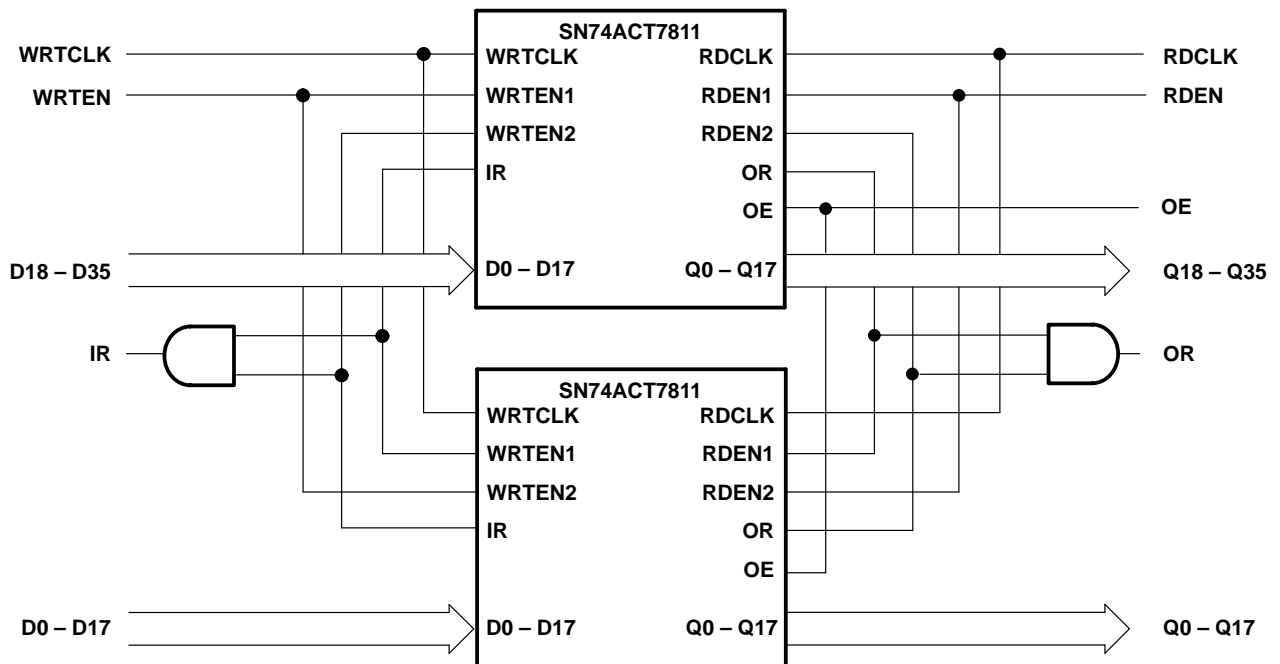


Figure 8. Word-Width Expansion: 1024 Words × 36 Bits

PARAMETER MEASUREMENT INFORMATION

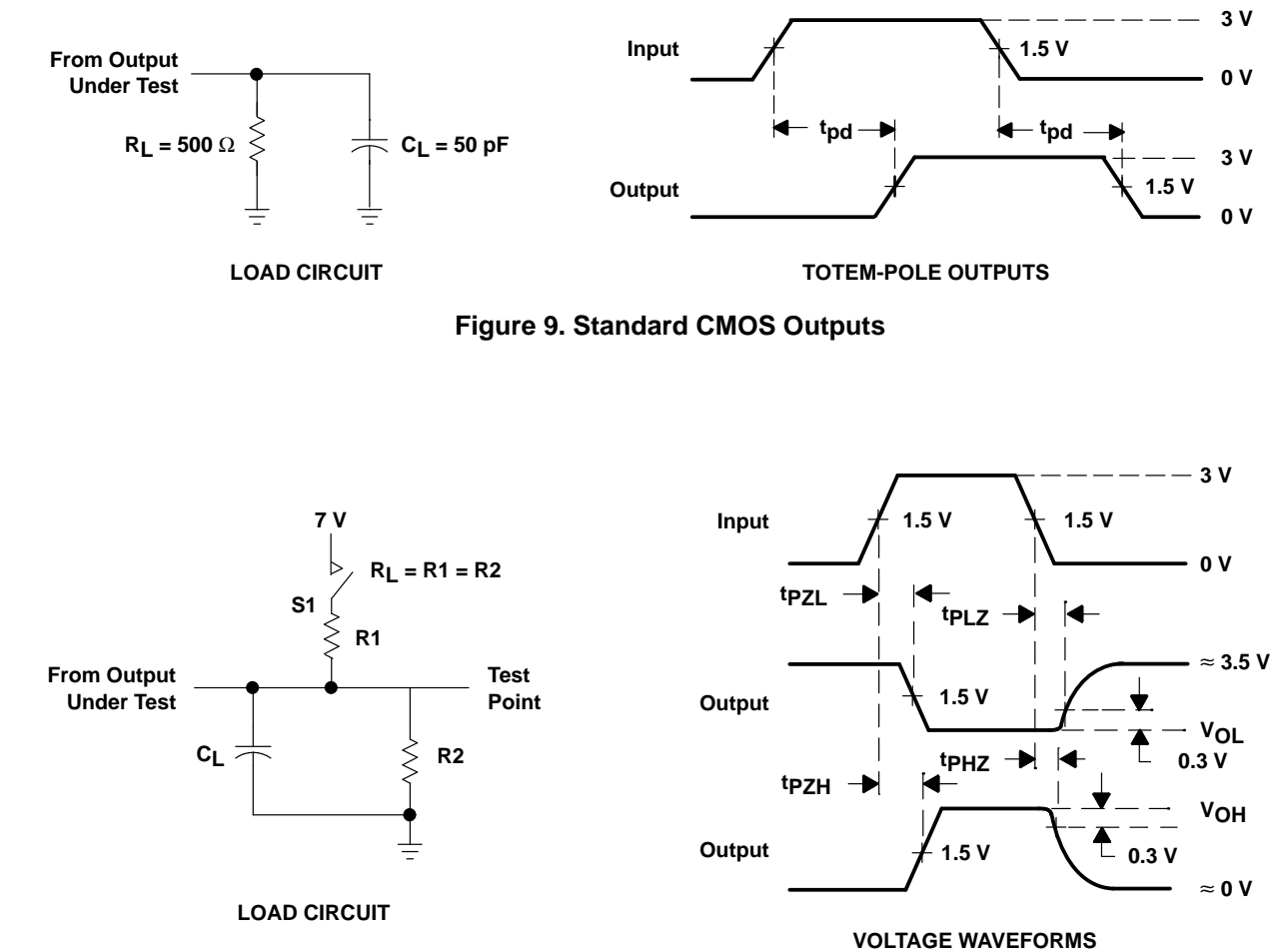


Figure 10. 3-State Outputs (Any Q)

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.