

54ACT11821, 74ACT11821 10-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCAS156A – NOVEMBER 1990 – REVISED APRIL 1993

- Inputs Are TTL-Voltage Compatible
- Provides Extra Data Width Necessary for Wider Address/Data Paths or Buses With Parity
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- μ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Ceramic 300-mil DIPs

description

These 10-bit flip-flops feature 3-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

On the positive transition of the clock the Q outputs will follow the D inputs.

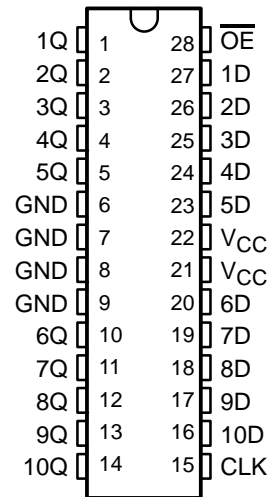
A buffered output enable (\overline{OE}) input can be used to place the ten outputs in either a normal logic state (high or low level) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

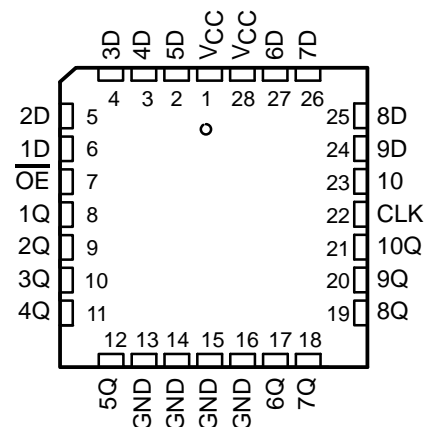
The output enable (\overline{OE}) does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The 54ACT11821 is characterized for operation over the full military temperature range of –55°C to 125°C. The 74ACT11821 is characterized for operation from –40°C to 85°C.

54ACT11821 . . . JT PACKAGE
74ACT11821 . . . DW PACKAGE
(TOP VIEW)



54ACT11821 . . . FK PACKAGE
(TOP VIEW)



EPIC is a trademark of Texas Instruments Incorporated.

UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1993, Texas Instruments Incorporated

54ACT11821, 74ACT11821

10-BIT BUS-INTERFACE FLIP-FLOPS

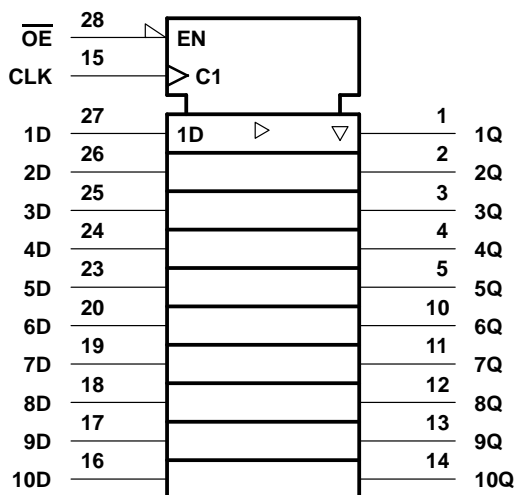
WITH 3-STATE OUTPUTS

SCAS156A – NOVEMBER 1990 – REVISED APRIL 1993

FUNCTION TABLE
(each flip-flop)

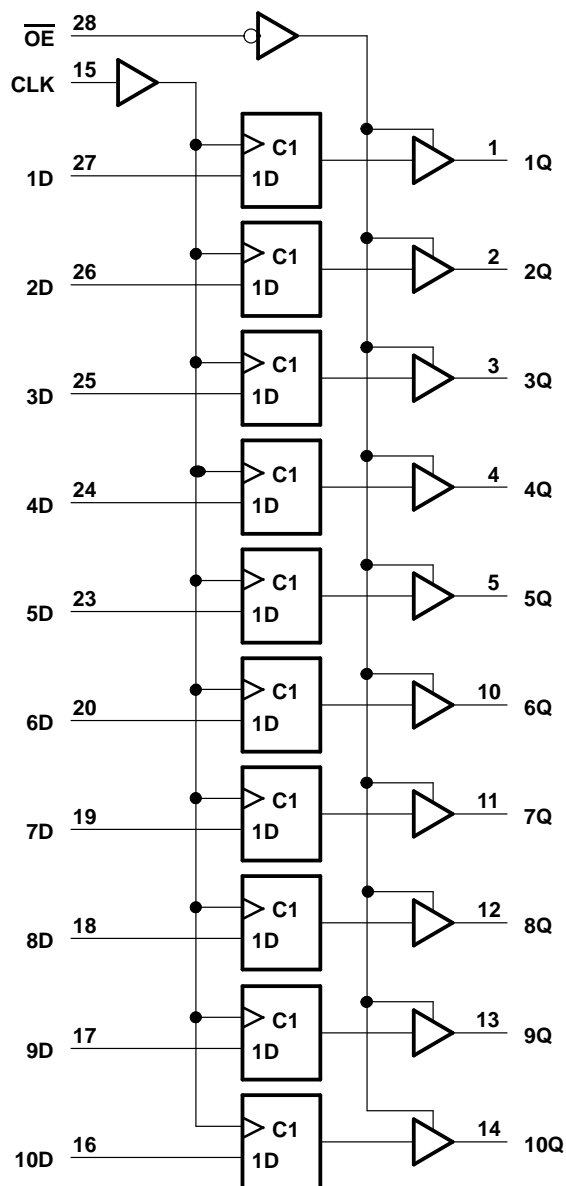
INPUTS			OUTPUT Q
\overline{OE}	CLK	D	
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
L	H	X	Q_0
L	↓	X	X_0
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Pin numbers shown are for the DW, JT, and NT packages.

54ACT11821, 74ACT11821
10-BIT BUS-INTERFACE FLIP-FLOPS
WITH 3-STATE OUTPUTS

SCAS156A – NOVEMBER 1990 – REVISED APRIL 1993

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND	±250 mA
Storage temperature range	–55°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		54ACT11821			74ACT11821			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current			–24			–24	mA
I_{OL}	Low-level output current			24			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10			10	ns/V
T_A	Operating free-air temperature	–55		125	–40		85	°C

NOTE 2: Unused or floating inputs must be held high or low.

54ACT11821, 74ACT11821

10-BIT BUS-INTERFACE FLIP-FLOPS

WITH 3-STATE OUTPUTS

SCAS156A – NOVEMBER 1990 – REVISED APRIL 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			54ACT11821		74ACT11821		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 µA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I _{OH} = -24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I _{OH} = -50 mA [†]	5.5 V				3.85				
	I _{OH} = -75 mA [†]	5.5 V						3.85		
V _{OL}	I _{OL} = 50 µA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I _{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I _{OL} = 50 mA [†]	5.5 V				1.65				
	I _{OL} = 75 mA [†]	5.5 V						1.65		
I _I	V _I = V _{CC} or GND	5.5 V			±0.1		±1		±1	µA
I _{OZ}	V _O = V _{CC} or GND	5.5 V			±0.5		±10		±5	µA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			8		160		80	µA
ΔI _{CC} [‡]	One input at 3.4 V, Other inputs at V _{CC} or GND	5.5 V			0.9		1		1	mA
C _i	V _I = V _{CC} or GND	5 V		4.5						pF
C _o	V _O = V _{CC} or GND	5 V		12						pF

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

[‡] This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

		T _A = 25°C		54ACT11821		74ACT11821		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency	0	125	0	125	0	125	MHz
t _w	Pulse duration, CLK high or low	4		4		4		ns
t _{su}	Setup time, data before CLK [↑]	2.5		2.5		2.5		ns
t _h	Hold time, data after CLK [↑]	1.5		1.5		1.5		ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T _A = 25°C			54ACT11821		74ACT11821		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f _{max}			125			125		125		MHz
t _{PLH}	CLK	Any Q	4.7	7.6	10.4	4.7	12.6	4.7	11.7	ns
t _{PHL}			5	8.1	11	5	12.9	5	12.1	
t _{PZH}	\overline{OE}	Any Q	3.1	6.1	9.1	3.1	10.8	3.1	10	ns
t _{PZL}			4.1	7.6	11	4.1	13.2	4.1	12.3	
t _{PHZ}	\overline{OE}	Any Q	4.8	7.2	9.2	4.8	10.6	4.8	10.1	ns
t _{PLZ}			4.8	6.8	8.6	4.8	9.8	4.8	9.4	

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



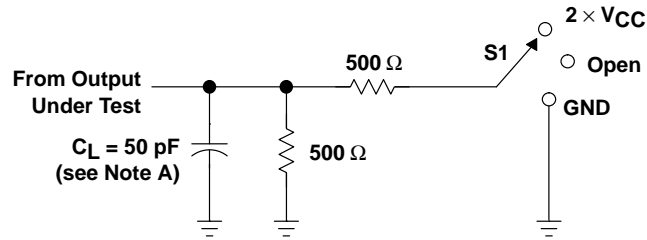
54ACT11821, 74ACT11821 10-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCAS156A – NOVEMBER 1990 – REVISED APRIL 1993

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

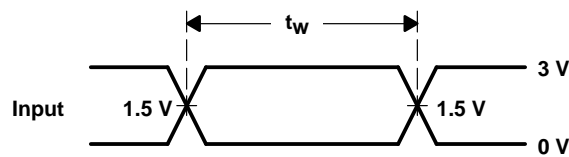
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per flip-flop	$C_L = 50\text{ pF}$, $f = 1\text{ MHz}$	45	pF
	Outputs enabled		31	

PARAMETER MEASUREMENT INFORMATION

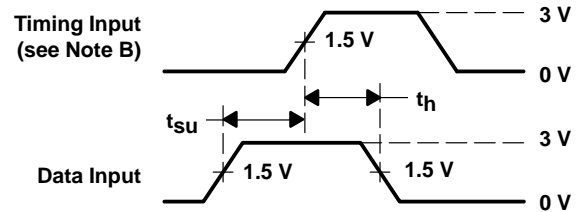


LOAD CIRCUIT

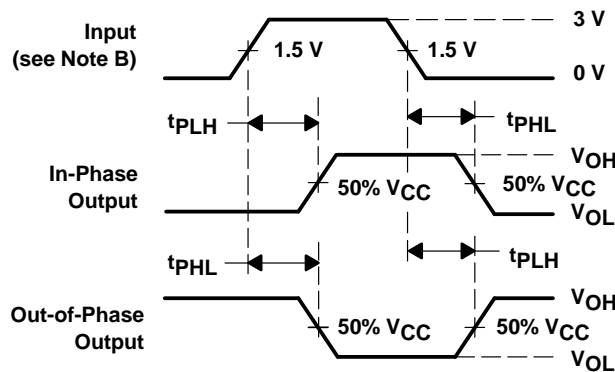
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	GND



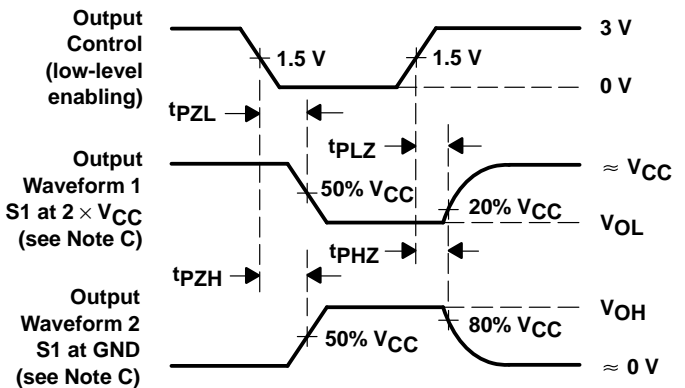
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$, $t_r = 3\text{ ns}$, $t_f = 3\text{ ns}$.

C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.