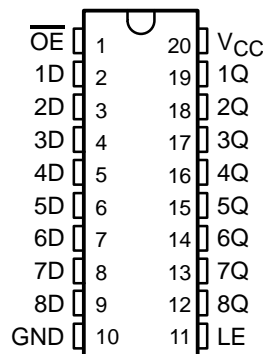


# SN74LVC573A OCTAL TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

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- **EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Typical  $V_{OLP}$  (Output Ground Bounce)**  
 $< 0.8\text{ V}$  at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$
- **Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot)**  
 $> 2\text{ V}$  at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$
- **Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V  $V_{CC}$ )**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model ( $C = 200\text{ pF}$ ,  $R = 0$ )**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages**

DB, DW, OR PW PACKAGE  
(TOP VIEW)



## description

This octal transparent D-type latch is designed for 2.7-V to 3.6-V  $V_{CC}$  operation; it can interface to a 5-V system environment.

The SN74LVC573A features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, input/output (I/O) ports, bidirectional bus drivers, and working registers.

While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels at the D inputs.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without the need for interface or pullup components.

$\overline{OE}$  does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVC573A is characterized for operation from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .



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**TEXAS  
INSTRUMENTS**

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SN74LVC573A

OCTAL TRANSPARENT D-TYPE LATCH

WITH 3-STATE OUTPUTS

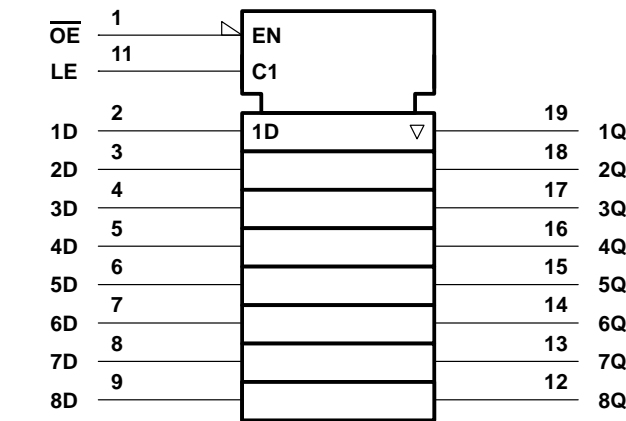
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FUNCTION TABLE

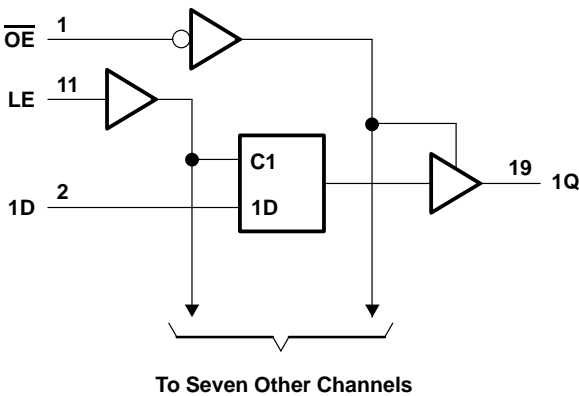
(each latch)

INPUTS			OUTPUT Q
$\overline{\text{OE}}$	LE	D	
L	H	H	H
L	H	L	L
L	L	X	$Q_0$
H	X	X	Z

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$	−0.5 V to 6.5 V
Input voltage range, $V_I$ (see Note 1)	−0.5 V to 6.5 V
Voltage range applied to any output in the high impedance state or power off state, $V_O$ (see Note 1)	−0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, $V_O$ (see Notes 1 and 2)	−0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	−50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ )	±50 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±50 mA
Continuous current through $V_{CC}$ or GND	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 3):	
DB package	0.6 W
DW package	1.6 W
PW package	0.7 W
Storage temperature range, $T_{stg}$	−65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This value is limited to 4.6 V maximum.

3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

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## OCTAL TRANSPARENT D-TYPE LATCH

### WITH 3-STATE OUTPUTS

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#### recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
$V_{CC}$	Supply voltage	Operating	2	3.6	V
		Data retention only	1.5		
$V_{IH}$	High-level input voltage	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	2		V
$V_{IL}$	Low-level input voltage	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$		0.8	V
$V_I$	Input voltage		0	5.5	V
$V_O$	Output voltage	High or low state	0	$V_{CC}$	V
		3 state	0	5.5	
$I_{OH}$	High-level output current	$V_{CC} = 2.7\text{ V}$		-12	mA
		$V_{CC} = 3\text{ V}$		-24	
$I_{OL}$	Low-level output current	$V_{CC} = 2.7\text{ V}$		12	mA
		$V_{CC} = 3\text{ V}$		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
$T_A$	Operating free-air temperature		-40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$V_{CC}^\dagger$	MIN	TYP <sup>‡</sup>	MAX	UNIT
$V_{OH}$	$I_{OH} = -100\text{ }\mu\text{A}$	MIN to MAX	$V_{CC}-0.2$			V
	$I_{OH} = -12\text{ mA}$	2.7 V	2.2			
		3 V	2.4			
	$I_{OH} = -24\text{ mA}$	3 V	2.2			
$V_{OL}$	$I_{OL} = 100\text{ }\mu\text{A}$	MIN to MAX			0.2	V
	$I_{OL} = 12\text{ mA}$	2.7 V			0.4	
	$I_{OL} = 24\text{ mA}$	3 V			0.55	
$I_I$	$V_I = 5.5\text{ V or GND}$	3.6 V			$\pm 5$	$\mu\text{A}$
$I_{OZ}$	$V_O = V_{CC}\text{ or GND}$	MIN to MAX			$\pm 10$	$\mu\text{A}$
	$V_O = 3.6\text{ V or }5.5\text{ V}$				$\pm 50$	
$I_{CC}$	$V_I = V_{CC}\text{ or GND, } I_O = 0$	3.6 V			10	$\mu\text{A}$
$\Delta I_{CC}$	One input at $V_{CC} - 0.6\text{ V}$ , Other inputs at $V_{CC}\text{ or GND}$	2.7 V to 3.6 V			500	$\mu\text{A}$
$C_i$	$V_I = V_{CC}\text{ or GND}$	3.3 V		3		pF
$C_o$	$V_O = V_{CC}\text{ or GND}$	3.3 V		3.5		pF

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

<sup>‡</sup> All typical values are measured at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

#### timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		UNIT
		MIN	MAX	MIN	MAX	
$t_W$	Pulse duration, LE high	3.3		3.3		ns
$t_{su}$	Setup time, data before LE $\downarrow$	2		2		ns
$t_h$	Hold time, data after LE $\downarrow$	1.5		1.5		ns



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## OCTAL TRANSPARENT D-TYPE LATCH

### WITH 3-STATE OUTPUTS

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switching characteristics over recommended operating free-air temperature range,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	
t <sub>pd</sub>	D	Q	1.5	7.5	8.5		ns
	LE		2	8.5	9.5		
t <sub>en</sub>	$\overline{OE}$	Q	1.5	7.5	8.5		ns
t <sub>dis</sub>	$\overline{OE}$	Q	1.5	7	8		ns
t <sub>sk(o)</sub> <sup>†</sup>			1				ns

$^\dagger$  Skew between any two outputs of the same package switching in the same direction. This parameter is warranted but not production tested.

operating characteristics,  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$

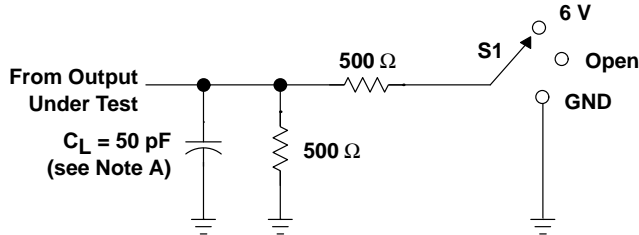
PARAMETER			TEST CONDITIONS	TYP	UNIT
$C_{pd}$	Power dissipation capacitance per latch	Outputs enabled	$C_L = 50$ pF, $f = 10$ MHz	20	pF
		Outputs disabled		3.5	



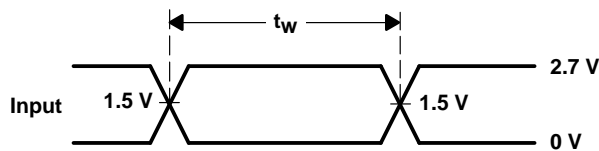
# SN74LVC573A OCTAL TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

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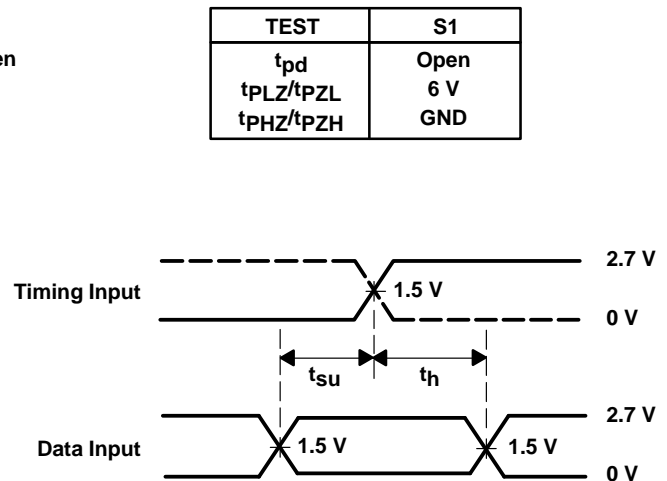
## PARAMETER MEASUREMENT INFORMATION



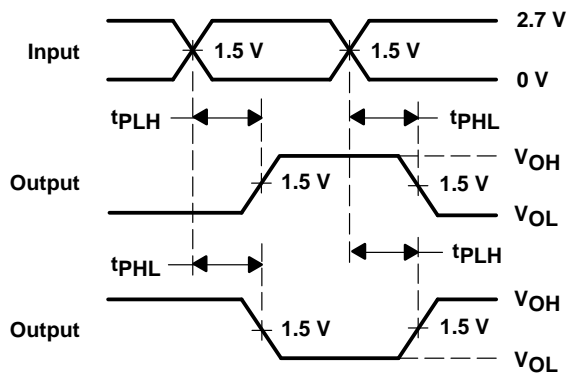
LOAD CIRCUIT FOR OUTPUTS



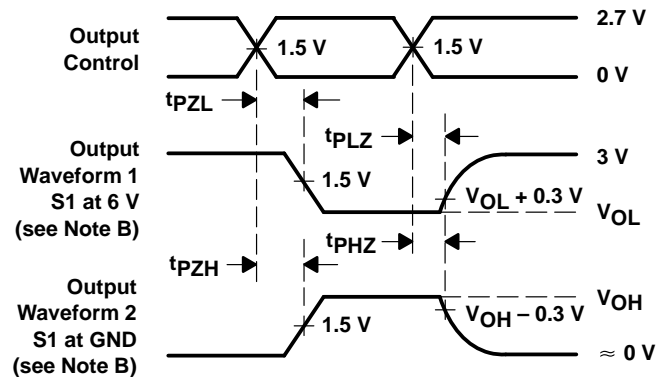
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns.
  - D. The outputs are measured one at a time with one transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

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