

SN74LVC823

9-BIT BUS-INTERFACE FLIP-FLOP WITH 3-STATE OUTPUTS

SCAS305A – MARCH 1993 – REVISED AUGUST 1995

- **EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Typical V_{OLP} (Output Ground Bounce) $< 0.8\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$**
- **Typical V_{OHV} (Output V_{OH} Undershoot) $> 2\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages**

description

This 9-bit bus-interface flip-flop is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC823 is designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

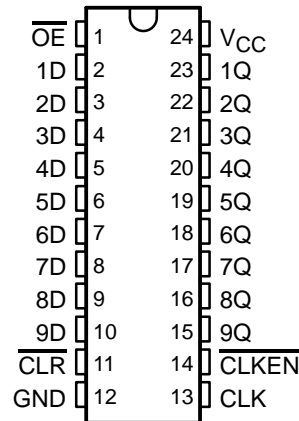
With the clock-enable ($\overline{\text{CLKEN}}$) input low, the nine D-type edge-triggered flip-flops enter data on the low-to-high transitions of the clock. Taking $\overline{\text{CLKEN}}$ high disables the clock buffer, latching the outputs. The SN74LVC823 has noninverting data (D) inputs. Taking the clear ($\overline{\text{CLR}}$) input low causes the nine Q outputs to go low independently of the clock.

A buffered output-enable ($\overline{\text{OE}}$) input can be used to place the nine outputs in either a normal logic state (high or low logic levels) or a high-impedance state. The output-enable ($\overline{\text{OE}}$) input does not affect the internal operations of the latch. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVC823 is characterized for operation from -40°C to 85°C .

DB, DW, OR PW PACKAGE
(TOP VIEW)



FUNCTION TABLE
(each flip-flop)

INPUTS					OUTPUT Q
$\overline{\text{OE}}$	$\overline{\text{CLR}}$	$\overline{\text{CLKEN}}$	CLK	D	
L	L	X	X	X	L
L	H	L	\uparrow	H	H
L	H	L	\uparrow	L	L
L	H	H	X	X	Q_0
H	X	X	X	X	Z



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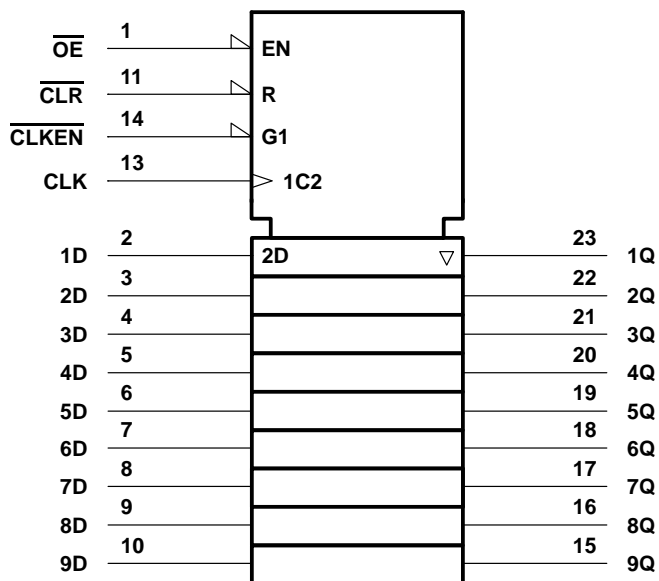
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WITH 3-STATE OUTPUTS

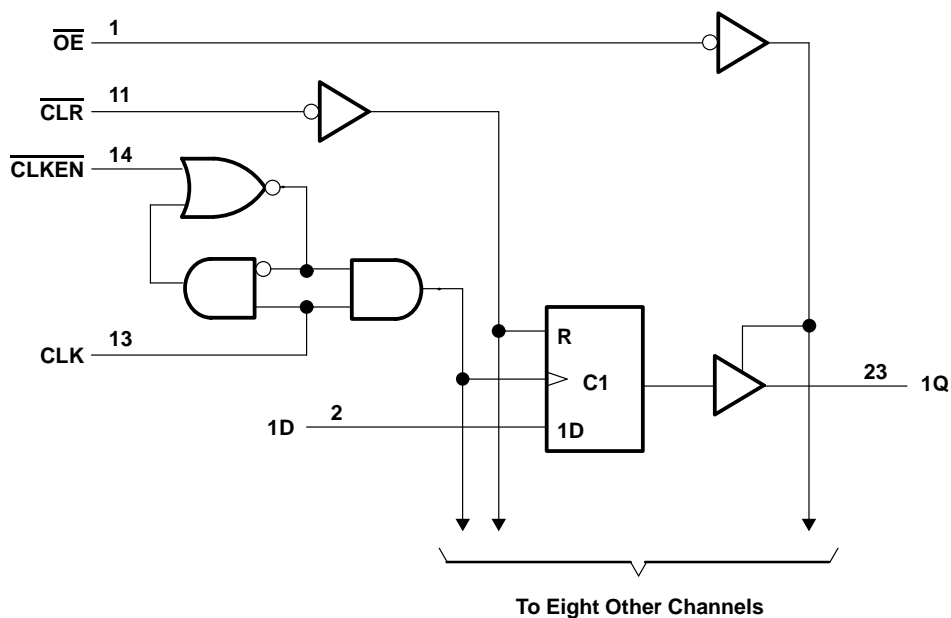
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 6.5 V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 3):	
DB package	0.65 W
DW package	1.7 W
PW package	0.7 W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7$ V to 3.6 V	2		V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		0.8	V
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2.7$ V		–12	mA
		$V_{CC} = 3$ V		–24	
I_{OL}	Low-level output current	$V_{CC} = 2.7$ V		12	mA
		$V_{CC} = 3$ V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		–40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC} †	MIN	TYP‡	MAX	UNIT
V _{OH}	I _{OH} = –100 µA	MIN to MAX	V _{CC} – 0.2			V
	I _{OH} = –12 mA	2.7 V	2.2			
		3 V	2.4			
	I _{OH} = –24 mA	3 V	2			
V _{OL}	I _{OL} = 100 µA	MIN to MAX	0.2			V
	I _{OL} = 12 mA	2.7 V	0.4			
	I _{OL} = 24 mA	3 V	0.55			
I _I	V _I = 5.5 V or GND	3.6 V	±5			µA
I _{OZ}	V _O = V _{CC} or GND	3.6 V	±10			µA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V	20			µA
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	3 V to 3.6 V	500			µA
C _i	V _I = V _{CC} or GND	3.3 V	9			pF
C _o	V _O = V _{CC} or GND	3.3 V	10			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

‡ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

timing characteristics over recommended operating free-air temperature range, (unless otherwise noted) (see Figure 1)

			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency		0	100	0	80	MHz
t _w	Pulse duration	CLR low	5		5		ns
		CLK high or low	4		4		
t _{su}	Setup time, data before CLK↑	CLR inactive	1		1		ns
		Data	2		3		
		CLKEN low	3.5		4.5		
t _h	Hold time, data after CLK↑	Data	2		2		ns
		CLKEN low	0.5		0.5		

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	
f _{max}			100		80		MHz
t _{pd}	CLK	Q	2	8	2	9	ns
	CLR	Q	1.5	8	1.5	9	
t _{en}	OE	Q	1.5	8.5	1.5	9.5	ns
t _{dis}	OE	Q	1.5	8	1.5	9	ns



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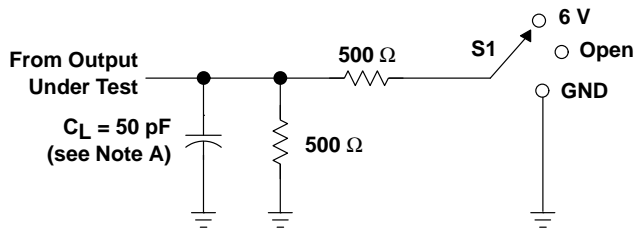
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operating characteristics, $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$

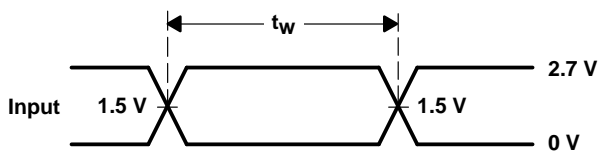
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per flip-flop	Outputs enabled	22	μF
		Outputs disabled	12	

PARAMETER MEASUREMENT INFORMATION

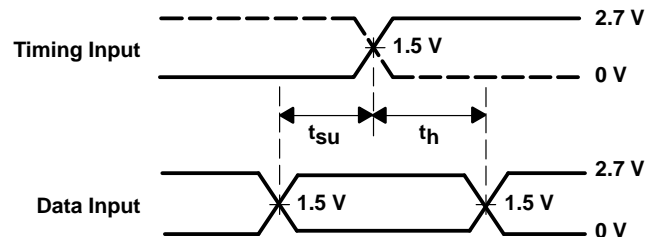


LOAD CIRCUIT FOR OUTPUTS

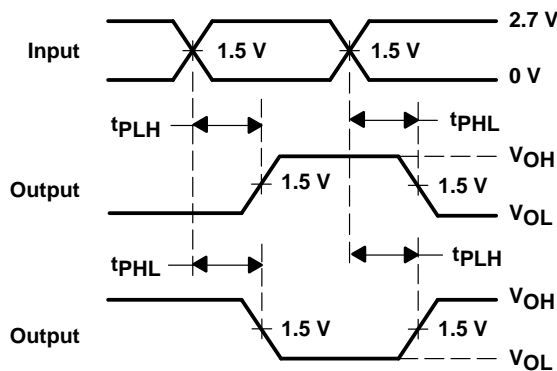
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



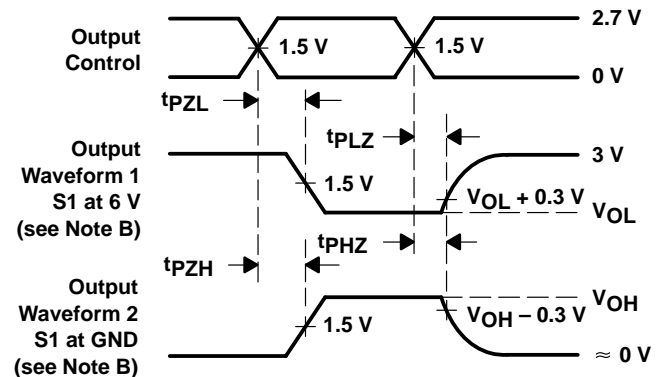
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms



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