

# SN54ACT74, SN74ACT74 DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH CLEAR AND PRESET

SCAS520C – AUGUST 1995 – REVISED SEPTEMBER 1996

- Inputs Are TTL-Voltage Compatible
- **EPIC™** (Enhanced-Performance Implanted CMOS) 1- $\mu$ m Process
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), DIP (N) Packages, Ceramic Chip Carrier (FK), DIP (J), and Flat (W) Packages

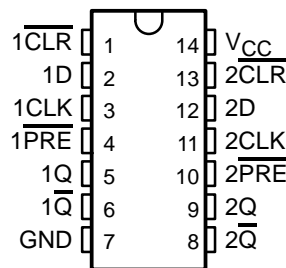
## description

The 'ACT74 are dual positive-edge-triggered D-type flip-flops.

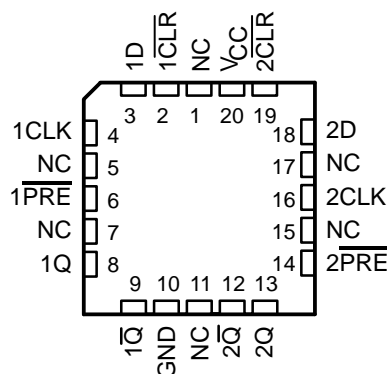
A low level at the preset ( $\overline{\text{PRE}}$ ) or clear ( $\overline{\text{CLR}}$ ) input sets or resets the outputs, regardless of the levels of the other inputs. When  $\overline{\text{PRE}}$  and  $\overline{\text{CLR}}$  are inactive (high), data at the data (D) input meeting the setup-time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at D can be changed without affecting the levels at the outputs.

The SN54ACT74 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74ACT74 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

**SN54ACT74 ... J OR W PACKAGE  
SN74ACT74 ... D, DB, N, OR PW PACKAGE  
(TOP VIEW)**



**SN54ACT74 ... FK PACKAGE  
(TOP VIEW)**



NC – No internal connection

**FUNCTION TABLE**

INPUTS				OUTPUTS	
$\overline{\text{PRE}}$	$\overline{\text{CLR}}$	CLK	D	Q	$\overline{\text{Q}}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H <sup>†</sup>	H <sup>†</sup>
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q <sub>0</sub>	$\overline{\text{Q}}_0$

<sup>†</sup> This configuration is unstable; that is, it does not persist when either  $\overline{\text{PRE}}$  or  $\overline{\text{CLR}}$  returns to its inactive (high) level.



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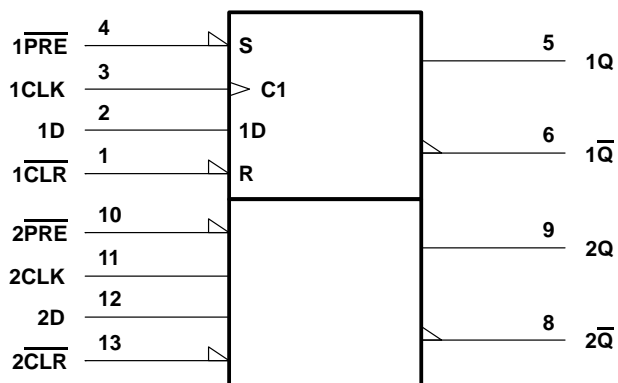
# SN54ACT74, SN74ACT74

## DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS

### WITH CLEAR AND PRESET

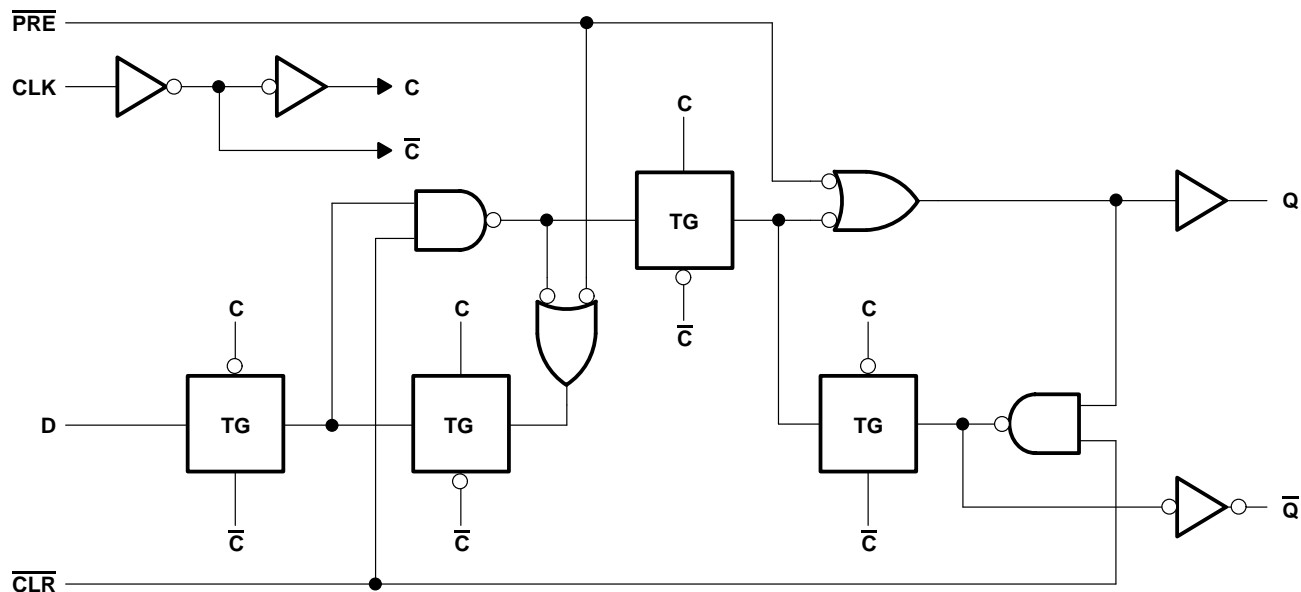
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#### logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.  
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

#### logic diagram, each flip-flop (positive logic)



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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, $V_O$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ )	±20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±50 mA
Continuous current through $V_{CC}$ or GND	±200 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2):	
D package	1.25 W
DB package	0.5 W
N package	1.1 W
PW package	0.5 W
Storage temperature range, $T_{stg}$	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

## recommended operating conditions (see Note 3)

		SN54ACT74		SN74ACT74		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	4.5	5.5	4.5	5.5	V
$V_{IH}$	High-level input voltage	2		2		V
$V_{IL}$	Low-level input voltage		0.8		0.8	V
$V_I$	Input voltage	0	$V_{CC}$	0	$V_{CC}$	V
$V_O$	Output voltage	0	$V_{CC}$	0	$V_{CC}$	V
$I_{OH}$	High-level output current		–24		–24	mA
$I_{OL}$	Low-level output current		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	8	0	8	ns/V
$T_A$	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.



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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54ACT74		SN74ACT74		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = –50 µA	4.5 V	4.4	4.49		4.4		4.4		V
		5.5 V	5.4	5.49		5.4		5.4		
	I <sub>OH</sub> = –24 mA	4.5 V	3.86			3.7		3.76		
		5.5 V	4.86			4.7		4.76		
	I <sub>OH</sub> = –50 mA <sup>†</sup>	5.5 V				3.86				
	I <sub>OH</sub> = –75 mA <sup>†</sup>	5.5 V						3.85		
V <sub>OL</sub>	I <sub>OL</sub> = 50 µA	4.5 V		0.001	0.1		0.1		0.1	V
		5.5 V		0.001	0.1		0.1		0.1	
	I <sub>OL</sub> = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I <sub>OL</sub> = 50 mA <sup>†</sup>	5.5 V					1.65			
	I <sub>OL</sub> = 75 mA <sup>†</sup>	5.5 V							1.65	
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V			±0.1		±1		±1	µA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			2		40		20	µA
ΔI <sub>CC</sub> <sup>‡</sup>	One input at 3.4 V, Other inputs at GND or V <sub>CC</sub>	5.5 V		0.6			1.6		1.5	µA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		3						pF

<sup>†</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed 2 ms.

<sup>‡</sup> This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V<sub>CC</sub>.

**timing characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)**

			T <sub>A</sub> = 25°C		SN54ACT74		SN74ACT74		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency		0	145	0	145	0	145	MHz
t <sub>w</sub>	Pulse duration	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ low	5		7		6		ns
		CLK	5		7		6		
t <sub>su</sub>	Setup time, data before CLK↑	Data	3		4		3.5		ns
		$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ inactive	0		0.5		0		
t <sub>h</sub>	Hold time, data after CLK↑		1		1		1		ns

**switching characteristics over recommended operating free-air temperature (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ACT74				UNIT	
			T <sub>A</sub> = 25°C			MIN		MAX
			MIN	TYP	MAX			
f <sub>max</sub>			145	210		85	MHz	
t <sub>PLH</sub>	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$	Q or $\overline{\text{Q}}$	1	5.5	9.5	1	11.5	ns
t <sub>PHL</sub>			1	6	10	1	12.5	
t <sub>PLH</sub>	CLK	Q or $\overline{\text{Q}}$	1	7.5	11	1	14	ns
t <sub>PHL</sub>			1	6	10	1	12	



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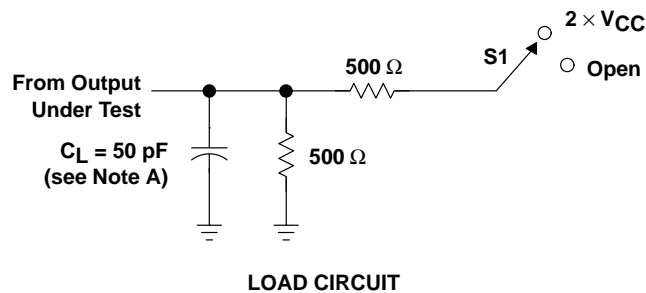
switching characteristics over recommended operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74ACT74					UNIT
			T <sub>A</sub> = 25°C			MIN	MAX	
			MIN	TYP	MAX			
f <sub>max</sub>			145	210		125		MHz
t <sub>PLH</sub>	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$	Q or $\overline{\text{Q}}$	3	5.5	9.5	2.5	10.5	ns
t <sub>PHL</sub>			3	6	10	3	11.5	
t <sub>PLH</sub>	CLK	Q or $\overline{\text{Q}}$	4	7.5	11	4	13	ns
t <sub>PHL</sub>			3.5	6	10	3	11.5	

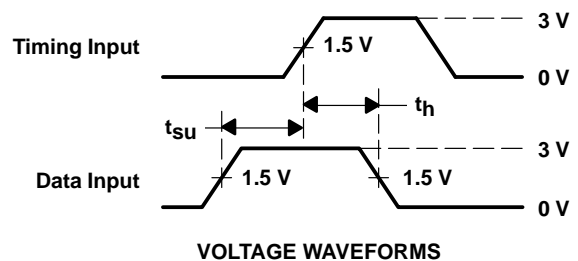
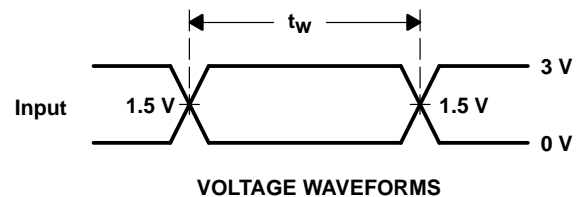
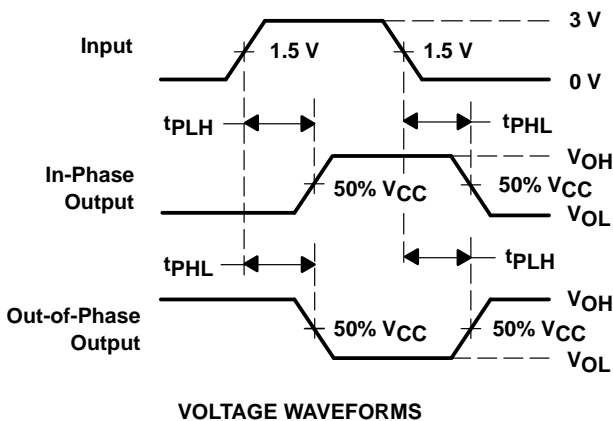
operating characteristics,  $V_{\text{CC}} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{\text{pd}}$ Power dissipation capacitance	$C_L = 50\text{ pF}$ , $f = 1\text{ MHz}$	45	pF

### PARAMETER MEASUREMENT INFORMATION



TEST	S1
$t_{\text{PLH}}/t_{\text{PHL}}$	Open



NOTES: A.  $C_L$  includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics:  $\text{PRR} \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2.5\text{ ns}$ ,  $t_f \leq 2.5\text{ ns}$ .

C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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