

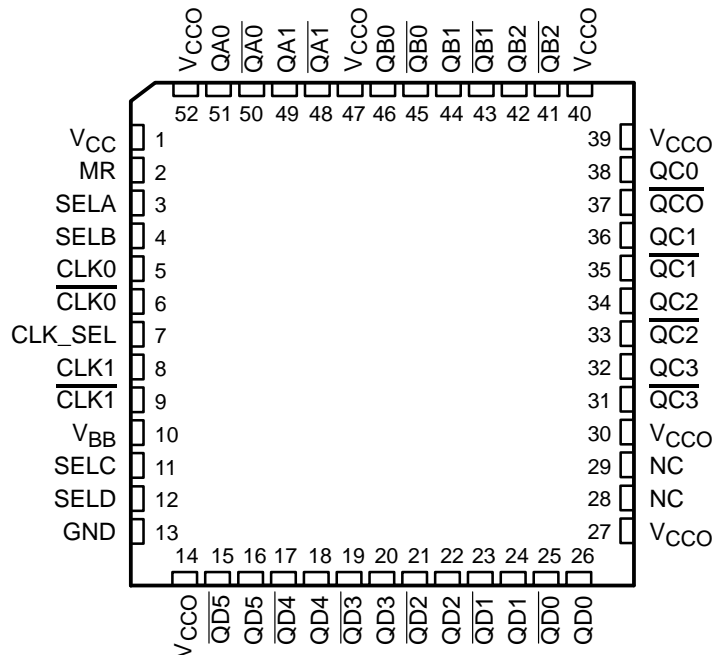
# CDC222

## 1-LINE TO 15-LINE DIFFERENTIAL CLOCK DRIVER

SCAS548A – NOVEMBER 1995 – REVISED JUNE 1996

- Low Output Skew for Clock-Distribution and Clock-Generation Applications
- Differential Low-Voltage Pseudo-ECL (LVPECL)-Compatible Inputs and Outputs
- Distributes Differential Clock Inputs to 15 Differential Clock Outputs
- Output Reference Voltage,  $V_{REF}$ , Allows Distribution From a Single-Ended Clock Input
- Outputs Configurable to Provide 1X or 1/2X Input Reference Frequency
- Single-Ended LVPECL-Compatible Output Enable
- Packaged in 52-Pin Thin Quad Flat Package

PAH PACKAGE  
(TOP VIEW)



NC – No internal connection

### description

The differential LVPECL clock-driver circuit distributes one pair of differential LVPECL clock inputs (CLKIN,  $\overline{\text{CLKIN}}$ ) to fifteen pairs of differential clock (Y,  $\overline{\text{Y}}$ ) outputs with minimum skew for clock distribution. It is specifically designed for driving 50- $\Omega$  transmission lines.

When the master reset (MR) input is in the low state, the 15 differential outputs switch at the same or one-half the frequency of the differential clock inputs. When MR is in the high state, the 15 differential outputs are forced to static states (Y outputs in the low state,  $\overline{\text{Y}}$  outputs in the high state), and the divide-by-two outputs are reset. MR is latched on the negative-edge of the CLKIN input so that the Q outputs are always disabled in the low state.

The four output banks are configured as a bank of two, a bank of three, a bank of four, and a bank of six. Each bank may be configured to provide either same-frequency or half-frequency outputs via the SEL inputs.

The voltage-reference ( $V_{BB}$ ) output can be strapped to  $\overline{\text{CLKIN}}$  for a single-ended CLKIN input.

The CDC222 is characterized for operation from 0°C to 70°C.



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PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

**TEXAS  
INSTRUMENTS**

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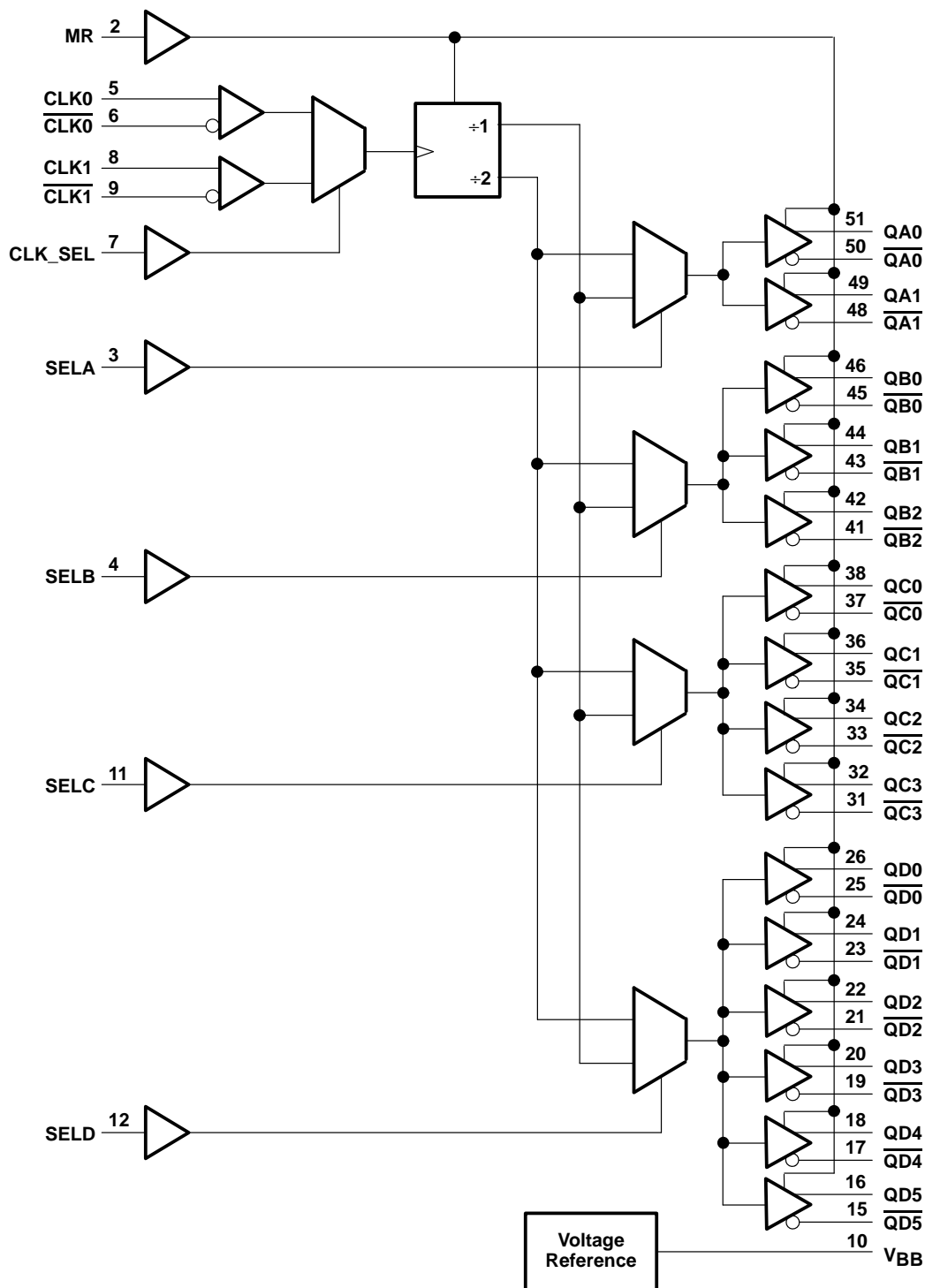
PRODUCT PREVIEW

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### logic diagram (positive logic)



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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$	–0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, $V_O$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–18 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	–18 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	–50mA
Continuous current through $V_{CC}$ or GND	±80mA
Maximum power dissipation at $T_A = 55^\circ$ (in still air) (see Note 2)	1.2 W
Storage temperature range, $T_{stg}$	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 75 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002.

### recommended operating conditions

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	3	3.6	V
$V_{IH}$	High-level input voltage	$V_{CC} = 3$ V to 3.6 V	$V_{CC} - 1.165$ $V_{CC} - 0.88$	V
		$V_{CC} = 3.3$ V	2.135 2.420	
$V_{IL}$	Low-level input voltage	$V_{CC} = 3$ V to 3.6 V	$V_{CC} - 1.81$ $V_{CC} - 1.475$	V
		$V_{CC} = 3.3$ V	1.490 1.825	
$f_{clock}$	Input clock frequency		500	MHz
$T_A$	Operating free-air temperature	0	70	°C

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
$V_{REF}$	$V_{CC} = 3$ V to 3.6 V	$V_{CC} - 1.38$ $V_{CC} - 1.26$		V
	$V_{CC} = 3.3$ V	1.925 2.075		
$V_{OH}$	$V_{CC} = 3$ V to 3.6 V	$V_{CC} - 1.025$ $V_{CC} - 0.88$		V
	$V_{CC} = 3.3$ V	2.275 2.42		
$V_{OL}$	$V_{CC} = 3$ V to 3.6 V	$V_{CC} - 1.81$ $V_{CC} - 1.62$		V
	$V_{CC} = 3.3$ V	1.49 1.68		
$I_I$	$V_I = 2.4$ V, $V_{CC} = 3.6$ V		150	μA
$I_{CC}$	$I_O = 0$ , $V_{CC} = 3.6$ V		110	mA

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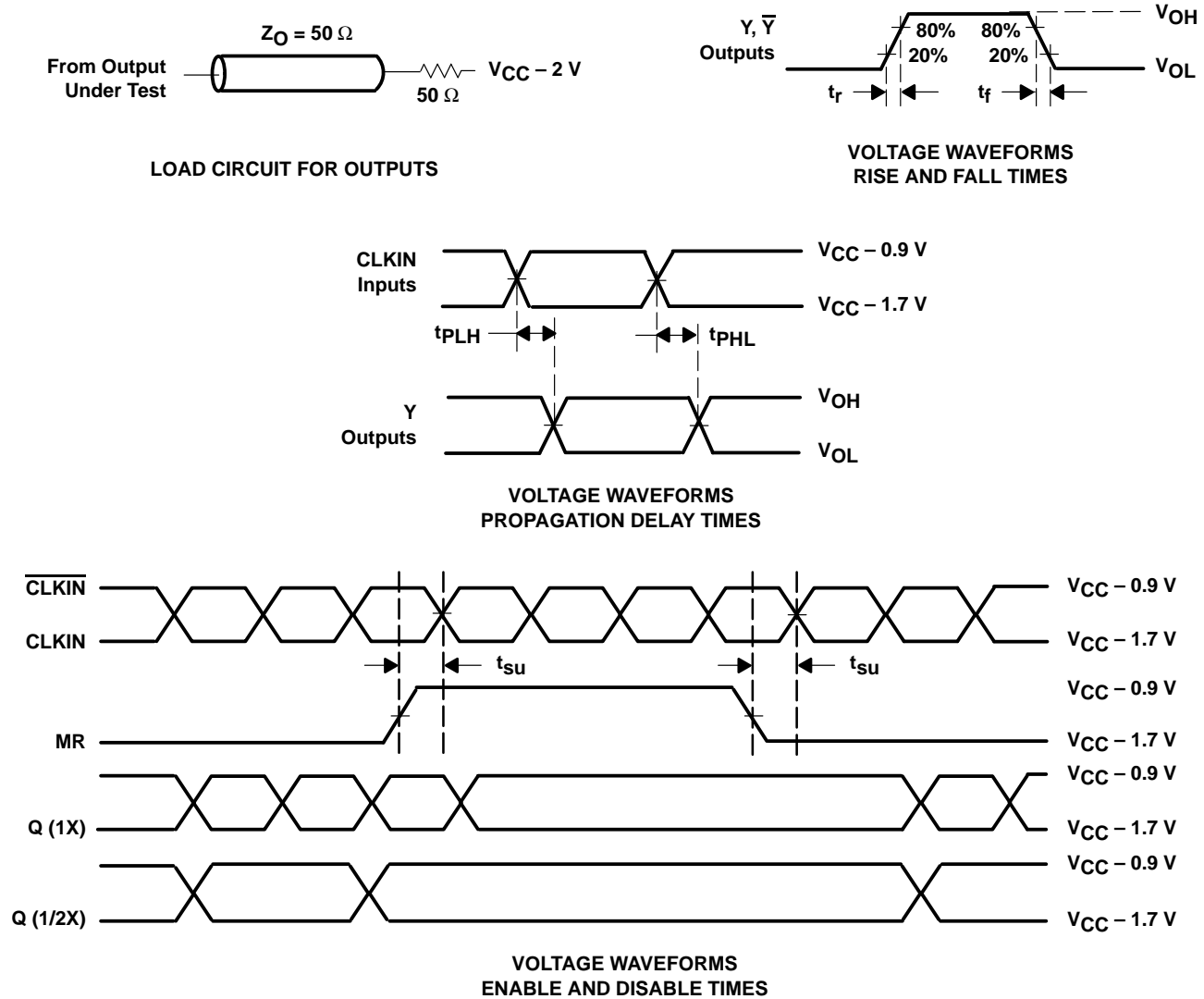
switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP	MAX	UNIT
$t_{PLH}$	CLKIN, $\overline{\text{CLKIN}}$	Q, $\overline{Q}$	0.9	1.0	1.1	ns
$t_{PHL}$			0.9	1.0	1.1	
$t_{su}$	MR $\uparrow$	CLKIN $\downarrow$				ns
$t_{sk(o)}$		Q, $\overline{Q}$			50	ps
$t_{sk(pr)}^{\dagger}$		Q, $\overline{Q}$			200	ps
$t_r$		Q, $\overline{Q}$			500	ps
$t_f$		Q, $\overline{Q}$			500	ps

$\dagger$  Process skew is valid only for devices operating at the same frequency, supply voltage, temperature, and output loading.

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### PARAMETER MEASUREMENT INFORMATION



- NOTES: A. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 45 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 1 \text{ ns}$ ,  $t_f \leq 1 \text{ ns}$ .  
 B. The outputs are measured one at a time with one transition per measurement.

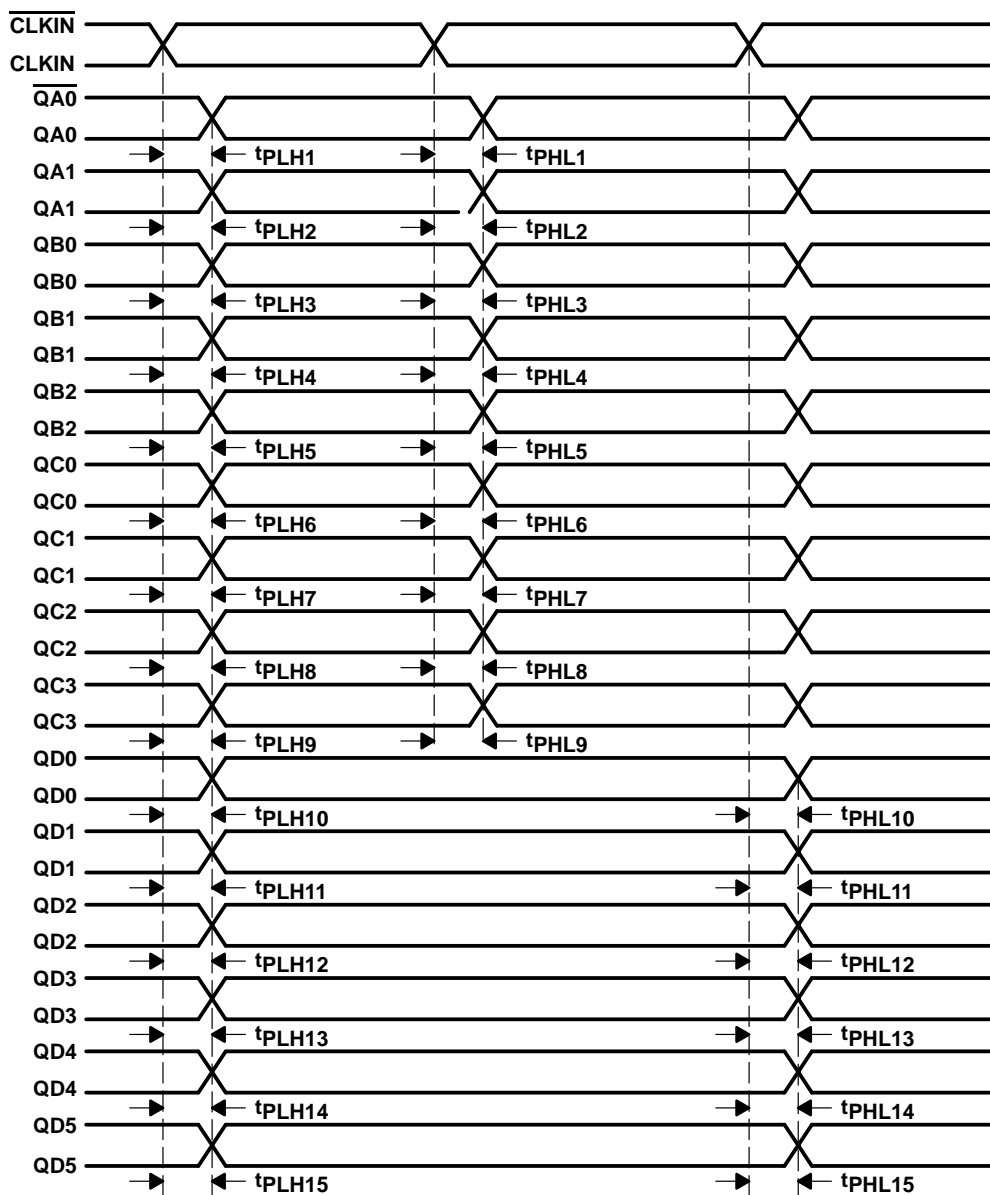
**Figure 1. Load Circuit and Voltage Waveforms**

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### PARAMETER MEASUREMENT INFORMATION



- NOTES: A. Output skew,  $t_{sk(o)}$ , is calculated as the greater of:
- The difference between the fastest and slowest  $t_{PLHn}$  ( $n = 1, 2, \dots, 15$ )
  - The difference between the fastest and slowest  $t_{PHLn}$  ( $n = 1, 2, \dots, 9$ )
  - The difference between the fastest and slowest  $t_{PHLn}$  ( $n = 10, 11, \dots, 15$ )
- B. Process skew,  $t_{sk(pr)}$ , is calculated as the greater of:
- The difference between the fastest and slowest  $t_{PLHn}$  ( $n = 1, 2, \dots, 9$ )
  - The difference between the fastest and slowest  $t_{PHLn}$  ( $n = 1, 2, \dots, 9$ )
  - The difference between the fastest and slowest  $t_{PHLn}$  ( $n = 10, 11, \dots, 15$ ) across multiple devices

Figure 2. Waveforms for Calculation of  $t_{sk(o)}$ ,  $t_{sk(pr)}$

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