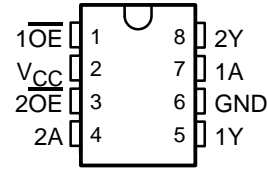


SN64BCT306 DUAL BUFFER/DRIVER WITH 3-STATE OUTPUTS

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- State-of-the-Art BiCMOS Design Significantly Reduces I_{CCZ}
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- High-Impedance State During Power Up and Power Down
- 3-State True Outputs Drive Bus Lines or Buffer-Memory Address Registers
- P-N-P Inputs Reduce DC Loading
- Package Options Include Plastic Small-Outline (D) Packages and Standard Plastic 300-mil DIPs (P)

D OR P PACKAGE
(TOP VIEW)



description

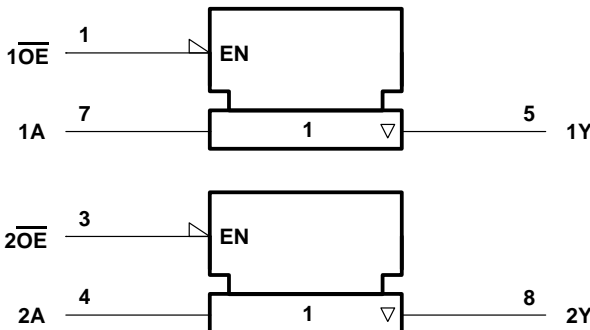
This dual buffer and line driver is designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The SN64BCT306 is characterized for operation from -40°C to 85°C and 0°C to 70°C .

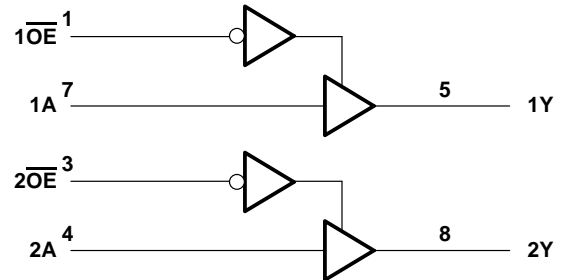
FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
$\overline{\text{OE}}$	A	Y
H	X	Z
L	L	L
L	H	H

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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DUAL BUFFER/DRIVER

WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the disabled or power-off state, V_O	–0.5 V to 5.5 V
Voltage range applied to any output in the high state, V_O	–0.5 V to V_{CC}
Input clamp current, I_{IK} ($V_I < 0$)	–30 mA
Current into any output in the low state, I_O	128 mA
Operating free-air temperature range	–40°C to 85°C
Storage temperature range	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input negative-voltage rating may be exceeded if the input clamp-current rating is observed.

recommended operating conditions (see Note 2)

	MIN	NOM	MAX	UNIT
V_{CC} Supply voltage	4.5	5	5.5	V
V_{IH} High-level input voltage	2			V
V_{IL} Low-level input voltage			0.8	V
I_{IK} Input clamp current			–18	mA
I_{OH} High-level output current			–15	mA
I_{OL} Low-level output current			64	mA
$\Delta t/\Delta V_{CC}$ Power-up ramp rate	2			$\mu s/V$
T_A Operating free-air temperature	–40		85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP [‡]	MAX	UNIT
V_{IK}	$V_{CC} = 4.5$ V,	$I_I = -18$ mA			–1.2	V
V_{OH}	$V_{CC} = 4.5$ V	$I_{OH} = -3$ mA	2.4	3.3		V
		$I_{OH} = -15$ mA	2	3.1		
V_{OL}	$V_{CC} = 4.5$ V,	$I_{OL} = 64$ mA		0.42	0.55	V
I_I	$V_{CC} = 5.5$ V,	$V_I = 7$ V			0.1	mA
I_{IH}	$V_{CC} = 5.5$ V,	$V_I = 2.7$ V			20	μA
I_{IL}	$V_{CC} = 5.5$ V,	$V_I = 0.5$ V			–1	mA
I_{OZ}	$V_{CC} = 0$ to 2.3 V (power up)	$V_O = 2.7$ V or 0.5 V, $\overline{OE} = 0.8$ V			± 50	μA
	$V_{CC} = 1.8$ to 0 V (power down)				± 50	
I_{OZH}	$V_{CC} = 5.5$ V,	$V_O = 2.7$ V			50	μA
I_{OZL}	$V_{CC} = 5.5$ V,	$V_O = 0.5$ V			–50	μA
I_{OS}^{\S}	$V_{CC} = 5.5$ V,	$V_O = 0$	–100		–225	mA
I_{CCL}	$V_{CC} = 5.5$ V,	Outputs open		53	80	mA
I_{CCH}	$V_{CC} = 5.5$ V,	Outputs open		23	40	mA
I_{CCZ}	$V_{CC} = 5.5$ V,	Outputs open		4	10	mA

[‡] All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ C$.

^{\S} Not more than one output should be tested at a time, and the duration of the test should not exceed one second.



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DUAL BUFFER/DRIVER
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switching characteristics over recommended range of supply voltage, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$		$T_A = -40^\circ\text{C}$ to 85°C		$T_A = 0^\circ\text{C}$ to 70°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1.2	4.4	0.9	5.3	0.7	5	ns
t_{PHL}			1.7	5	1.4	6	1.4	5.5	
t_{PZH}	$\overline{1OE}$ or $\overline{2OE}$	Y	2	7.8	2	9	2	8.7	ns
t_{PZL}			2	8.1	2	9.4	2	8.9	
t_{PHZ}	$\overline{1OE}$ or $\overline{2OE}$	Y	2	6.7	2	8	2	7.7	ns
t_{PLZ}			2	7.6	2	9.8	2	8.9	

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

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