

# SN54ABT16500B, SN74ABT16500B 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS057E – DECEMBER 1990 – REVISED JULY 1994

- **Members of the Texas Instruments Widebus™ Family**
- **State-of-the-Art EPIC-II<sup>™</sup> BiCMOS Design Significantly Reduces Power Dissipation**
- **UBT™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V<sub>OLP</sub> (Output Ground Bounce) < 0.8 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

## description

These 18-bit universal bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

Data flow in each direction is controlled by output-enable (OEAB and  $\overline{\text{OEBA}}$ ), latch-enable (LEAB and LEBA), and clock ( $\overline{\text{CLKAB}}$  and  $\overline{\text{CLKBA}}$ ) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if  $\overline{\text{CLKAB}}$  is held at a high or low logic level. If LEAB is low, the A bus data is stored in the latch/flip-flop on the high-to-low transition of  $\overline{\text{CLKAB}}$ . Output-enable OEAB is active-high. When OEAB is high, the outputs are active. When OEAB is low, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses  $\overline{\text{OEBA}}$ , LEBA, and  $\overline{\text{CLKBA}}$ . The output enables are complementary (OEAB is active high and  $\overline{\text{OEBA}}$  is active low).

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The SN74ABT16500B is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT16500B is characterized over the full military temperature range of –55°C to 125°C. The SN74ABT16500B is characterized for operation from –40°C to 85°C.

SN54ABT16500B . . . WD PACKAGE  
SN74ABT16500B . . . DGG OR DL PACKAGE  
(TOP VIEW)

OEAB	1	56	GND
LEAB	2	55	$\overline{\text{CLKAB}}$
A1	3	54	B1
GND	4	53	GND
A2	5	52	B2
A3	6	51	B3
V <sub>CC</sub>	7	50	V <sub>CC</sub>
A4	8	49	B4
A5	9	48	B5
A6	10	47	B6
GND	11	46	GND
A7	12	45	B7
A8	13	44	B8
A9	14	43	B9
A10	15	42	B10
A11	16	41	B11
A12	17	40	B12
GND	18	39	GND
A13	19	38	B13
A14	20	37	B14
A15	21	36	B15
V <sub>CC</sub>	22	35	V <sub>CC</sub>
A16	23	34	B16
A17	24	33	B17
GND	25	32	GND
A18	26	31	B18
$\overline{\text{OEBA}}$	27	30	$\overline{\text{CLKBA}}$
LEBA	28	29	GND

Widebus, EPIC-II<sup>™</sup>, and UBT are trademarks of Texas Instruments Incorporated.

UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1994, Texas Instruments Incorporated

# SN54ABT16500B, SN74ABT16500B

## 18-BIT UNIVERSAL BUS TRANSCEIVERS

### WITH 3-STATE OUTPUTS

SCBS057E – DECEMBER 1990 – REVISED JULY 1994

FUNCTION TABLE†

INPUTS				OUTPUT B
OEAB	LEAB	CLKAB	A	
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↓	L	L
H	L	↓	H	H
H	L	H	X	B <sub>0</sub> ‡
H	L	L	X	B <sub>0</sub> §

† A-to-B data flow is shown: B-to-A flow is similar but uses OEBA, LEBA, and CLKBA.

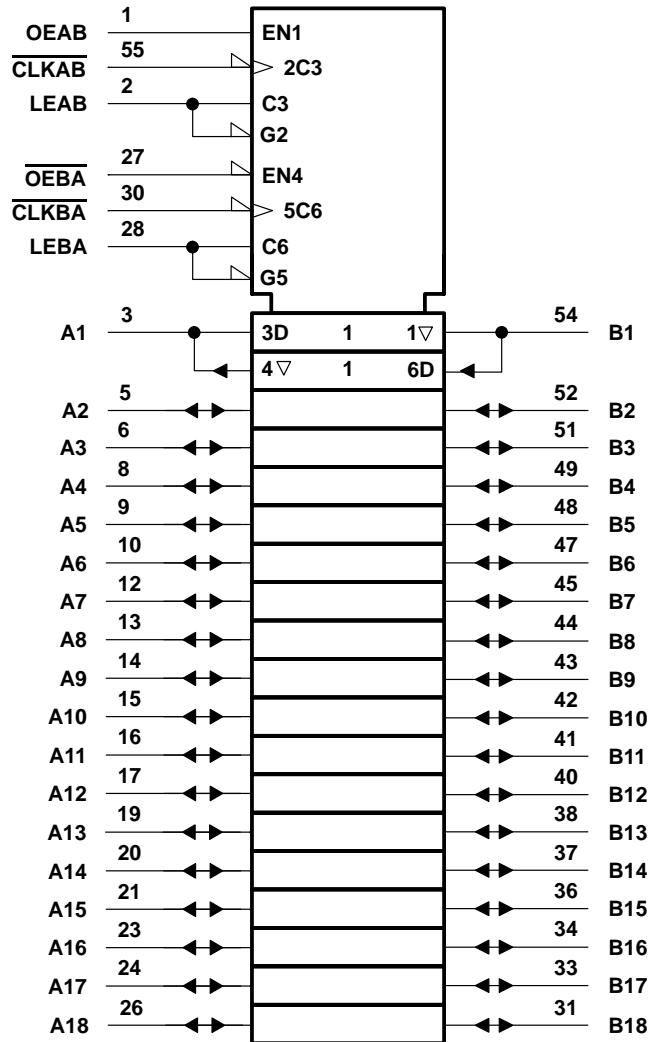
‡ Output level before the indicated steady-state input conditions were established.

§ Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low.

SN54ABT16500B, SN74ABT16500B  
18-BIT UNIVERSAL BUS TRANSCEIVERS  
WITH 3-STATE OUTPUTS

SCBS057E – DECEMBER 1990 – REVISED JULY 1994

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

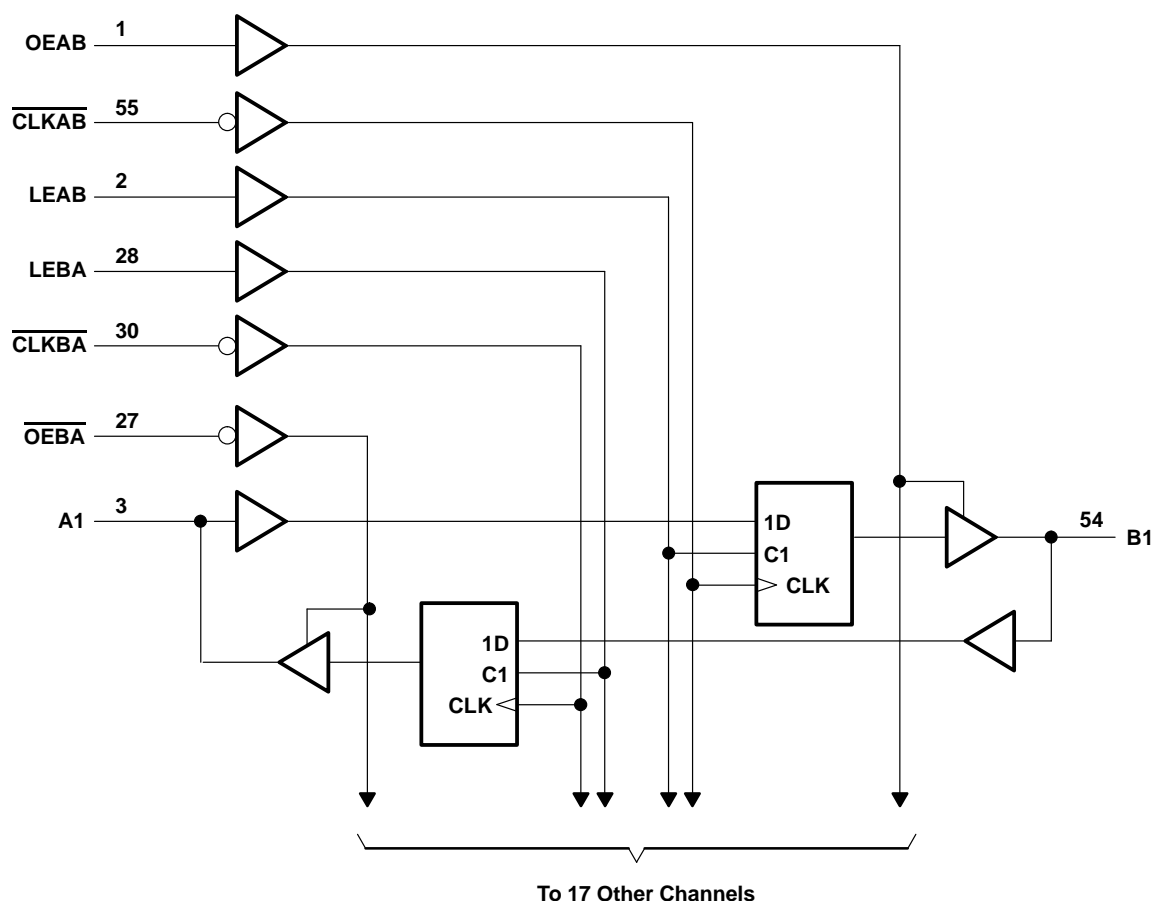
# SN54ABT16500B, SN74ABT16500B

## 18-BIT UNIVERSAL BUS TRANSCEIVERS

### WITH 3-STATE OUTPUTS

SCBS057E – DECEMBER 1990 – REVISED JULY 1994

#### logic diagram (positive logic)



#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (except I/O ports) (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, $V_O$	–0.5 V to 5.5 V
Current into any output in the low state, $I_O$ : SN54ABT16500B	96 mA
SN74ABT16500B	128 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–18 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ )	–50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2): DGG package	1 W
DL package	1.4 W
Storage temperature range	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

# SN54ABT16500B, SN74ABT16500B 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS057E – DECEMBER 1990 – REVISED JULY 1994

## recommended operating conditions (see Note 3)

		SN54ABT16500B		SN74ABT16500B		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	4.5	5.5	4.5	5.5	V
$V_{IH}$	High-level input voltage	2		2		V
$V_{IL}$	Low-level input voltage		0.8		0.8	V
$V_I$	Input voltage	0	$V_{CC}$	0	$V_{CC}$	V
$I_{OH}$	High-level output current		–24		–32	mA
$I_{OL}$	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		$\mu s/V$
$T_A$	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused or floating pins (input or I/O) must be held high or low.

# SN54ABT16500B, SN74ABT16500B

## 18-BIT UNIVERSAL BUS TRANSCEIVERS

### WITH 3-STATE OUTPUTS

SCBS057E – DECEMBER 1990 – REVISED JULY 1994

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	T <sub>A</sub> = 25°C			SN54ABT16500B		SN74ABT16500B		UNIT	
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX		
V <sub>IK</sub>		V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = –18 mA	–1.2			–1.2		–1.2		V	
V <sub>OH</sub>		V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = – 3 mA	2.5			2.5		2.5		V	
		V <sub>CC</sub> = 5 V, I <sub>OH</sub> = – 3 mA	3			3		3			
		V <sub>CC</sub> = 4.5 V	I <sub>OH</sub> = – 24 mA	2			2				
			I <sub>OH</sub> = – 32 mA	2*					2		
V <sub>OL</sub>		V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 48 mA	0.55			0.55		V		
			I <sub>OL</sub> = 64 mA	0.55*			0.55				
I <sub>off</sub>		V <sub>CC</sub> = 0, V <sub>I</sub> or V <sub>O</sub> ≤ 4.5 V	±100					±100		μA	
I <sub>CEX</sub>	Outputs high	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 5.5 V	50			50		50		μA	
I <sub>I</sub>	Control inputs	V <sub>CC</sub> = 0 to 5.5 V, V <sub>I</sub> = V <sub>CC</sub> or GND	±1			±1		±1		μA	
	A or B ports	V <sub>CC</sub> = 2.1 V to 5.5 V, V <sub>I</sub> = V <sub>CC</sub> or GND	±20			±20		±20			
I <sub>O</sub> ‡		V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.5 V	–50	–100	–180	–50	–180	–50	–180	mA	
I <sub>OZPU</sub>		V <sub>CC</sub> = 0 to 2.1 V, V <sub>O</sub> = 0.5 to 2.7 V, $\overline{\text{OE}}$ or OE= X	±50			±50		±50		μA	
I <sub>OZPD</sub>		V <sub>CC</sub> = 2.1 V to 0, V <sub>O</sub> = 0.5 to 2.7 V, $\overline{\text{OE}}$ or OE= X	±50			±50		±50		μA	
I <sub>OZH</sub> §		V <sub>CC</sub> = 2.1 V to 5.5 V, V <sub>O</sub> = 2.7 V, $\overline{\text{OE}} \geq 2$ V, OE ≤ 0.8 V¶	10			10		10		μA	
I <sub>OZL</sub> §		V <sub>CC</sub> = 2.1 V to 5.5 V, V <sub>O</sub> = 0.5 V, $\overline{\text{OE}} \geq 2$ V, OE ≤ 0.8 V¶	–10			–10		–10		μA	
I <sub>CC</sub>	A or B ports	V <sub>CC</sub> = 5.5 V, I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND	Outputs high		3	3		3		mA	
			Outputs low		36	36		36			
			Outputs disabled		3	3		3			
ΔI <sub>CC</sub> #		V <sub>CC</sub> = 5.5V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND	50			50		50		μA	
C <sub>i</sub>	Control inputs	V <sub>I</sub> = 2.5 V or 0.5 V	3							pF	
C <sub>io</sub>	A or B ports	V <sub>O</sub> = 2.5 V or 0.5 V	9							pF	

\* On products compliant to MIL-STD-883, Class B, this parameter does not apply.

† All typical values are at V<sub>CC</sub> = 5 V.

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

§ The parameters I<sub>OZH</sub> and I<sub>OZL</sub> include the input leakage current.

¶ For V<sub>CC</sub> between 2.1 V and 4 V, OE should be less than or equal to 0.5 V to ensure a low state.

# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

# SN54ABT16500B, SN74ABT16500B

## 18-BIT UNIVERSAL BUS TRANSCEIVERS

### WITH 3-STATE OUTPUTS

SCBS057E – DECEMBER 1990 – REVISED JULY 1994

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

				SN54ABT16500B		SN74ABT16500B		UNIT
				MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency			0	150	0	150	MHz
t <sub>w</sub> <sup>†</sup>	Pulse duration	LEAB or LEBA high		2.5		2.5		ns
		CLKAB or CLKBA high or low		3		3		
t <sub>su</sub>	Setup time	A before CLKAB↓		3		3		ns
		B before CLKBA↓		3		3		
		A before LEAB↓ or B before LEBA↓	CLK high	1		1		
			CLK low	2.5		2.5		
t <sub>h</sub>	Hold time	A after CLKAB↓ or B after CLKBA↓		0		0		ns
		A after LEAB↓ or B after LEBA↓		2		2		

$^\dagger$  This parameter is specified by design but not tested.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$			SN54ABT16500B		SN74ABT16500B		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{\text{max}}$			150	200		150		150		MHz
$t_{\text{PLH}}$	A or B	B or A	1	2.5	3.6	1	4.2	1	4	ns
$t_{\text{PHL}}$			1	3.2	4.5	1	5.1	1	4.9	
$t_{\text{PLH}}$	LEAB or LEBA	B or A	1	3.2	4.5	1	5.6	1	5	ns
$t_{\text{PHL}}$			1	3.4	4.5	1	5.4	1	5	
$t_{\text{PLH}}$	$\overline{\text{CLKAB}}$ or $\overline{\text{CLKBA}}$	B or A	1	3.5	4.7	1	5.4	1	5.3	ns
$t_{\text{PHL}}$			1	3.5	4.7	1	5.4	1	5.3	
$t_{\text{PZH}}$	OEAB or $\overline{\text{OEBA}}$	B or A	1	3.4	4.6	1	5.3	1	5.1	ns
$t_{\text{PZL}}$			1.5	3.8	4.7	1.5	5.6	1.5	5.4	
$t_{\text{PHZ}}$	OEAB or $\overline{\text{OEBA}}$	B or A	1.5	4.5	5.7	1.5	6.9	1.5	6.5	ns
$t_{\text{PLZ}}$			1.4	3.4	4.7	1.4	5.8	1.4	5.4	

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

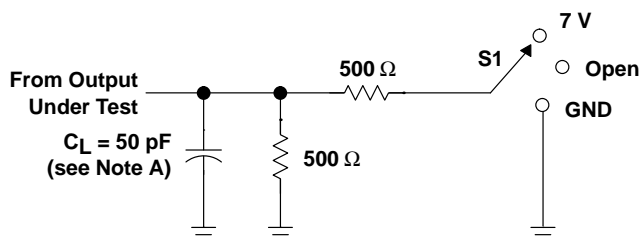
# SN54ABT16500B, SN74ABT16500B

## 18-BIT UNIVERSAL BUS TRANSCEIVERS

### WITH 3-STATE OUTPUTS

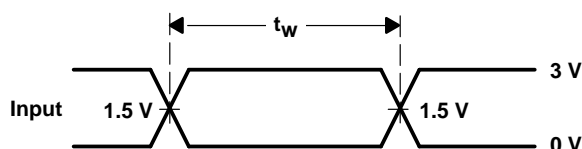
SCBS057E – DECEMBER 1990 – REVISED JULY 1994

#### PARAMETER MEASUREMENT INFORMATION

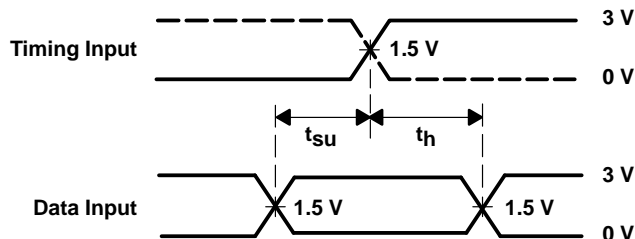


LOAD CIRCUIT FOR OUTPUTS

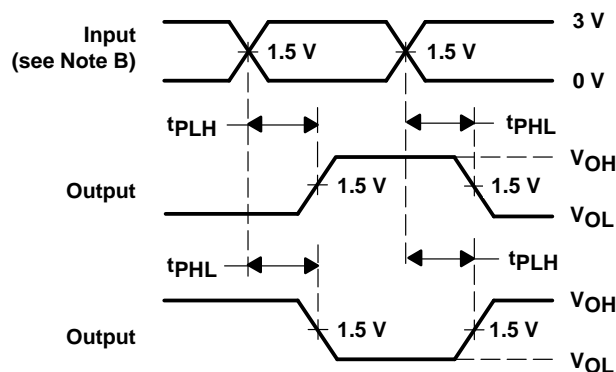
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	7 V
$t_{PHZ}/t_{PZH}$	Open



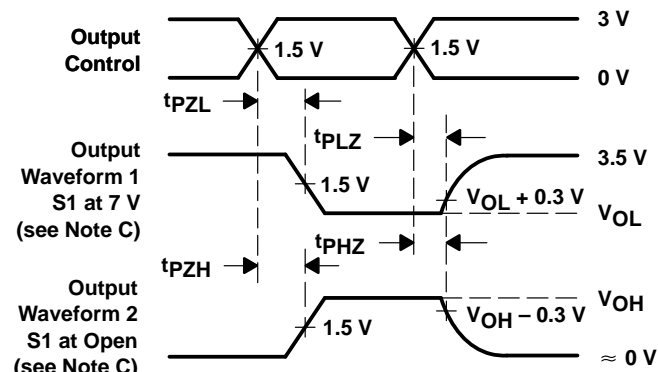
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns.  
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



## **IMPORTANT NOTICE**

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

**TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.**

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.