

SN54ABT2244A, SN74ABT2244A OCTAL BUFFERS AND LINE/MOS DRIVERS WITH 3-STATE OUTPUTS

SCBS106C – JANUARY 1991 – REVISED MARCH 1996

- Output Ports Have Equivalent 25- Ω Series Resistors, So No External Resistors Are Required
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- State-of-the-Art *EPIC-II B*[™] BiCMOS Design Significantly Reduces Power Dissipation
- Typical V_{OLP} (Output Ground Bounce) < 1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), and Plastic (N) and Ceramic (J) DIPs, and Ceramic Flat (W) Packages

description

These octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the 'ABT2240 and 'ABT2241, these devices provide the choice of selected combinations of inverting and noninverting outputs, symmetrical active-low output-enable (\overline{OE}) inputs, and complementary OE and \overline{OE} inputs. These devices feature high fan-out and improved fan-in.

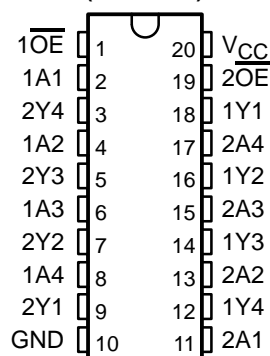
The outputs, which are designed to sink up to 12 mA, include 25- Ω series resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

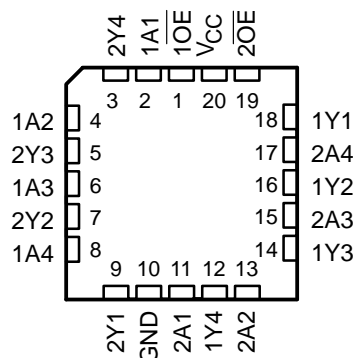
The SN74ABT2244A is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54ABT2244A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ABT2244A is characterized for operation from -40°C to 85°C .

SN54ABT2244A . . . J OR W PACKAGE
SN74ABT2244A . . . DB, DW, N, OR PW
PACKAGE
(TOP VIEW)



SN54ABT2244A . . . FK PACKAGE
(TOP VIEW)



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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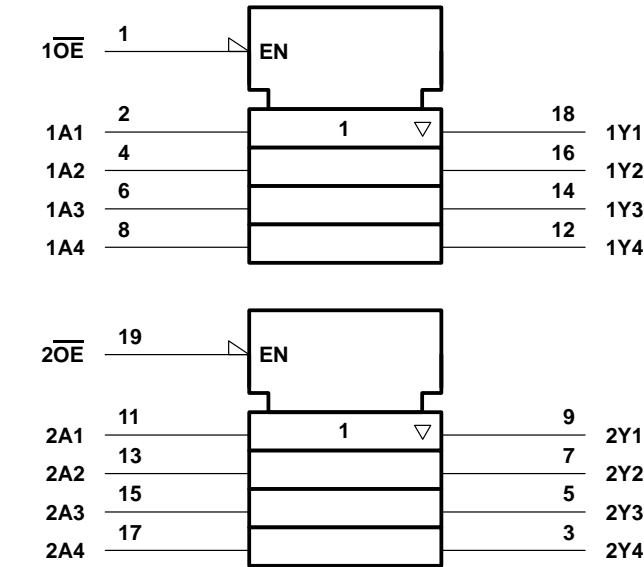
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SCBS106C – JANUARY 1991 – REVISED MARCH 1996

FUNCTION TABLE
(each buffer)

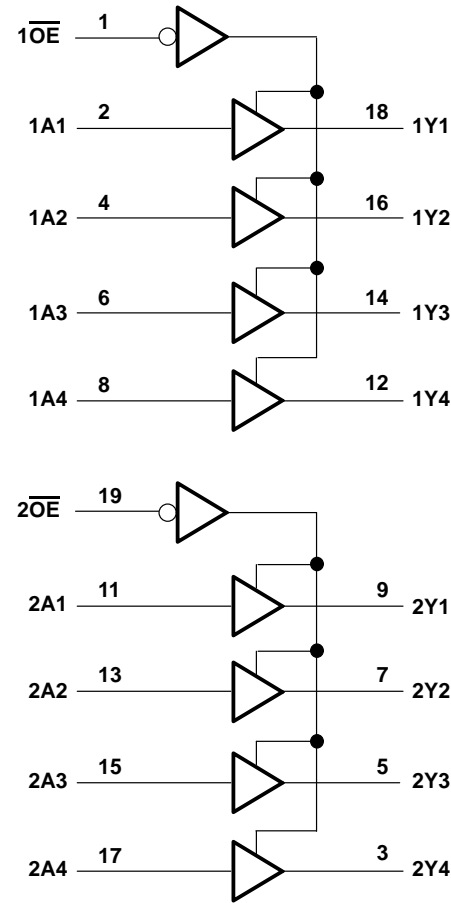
INPUTS		OUTPUT Y
\overline{OE}	A	
L	H	H
L	L	L
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

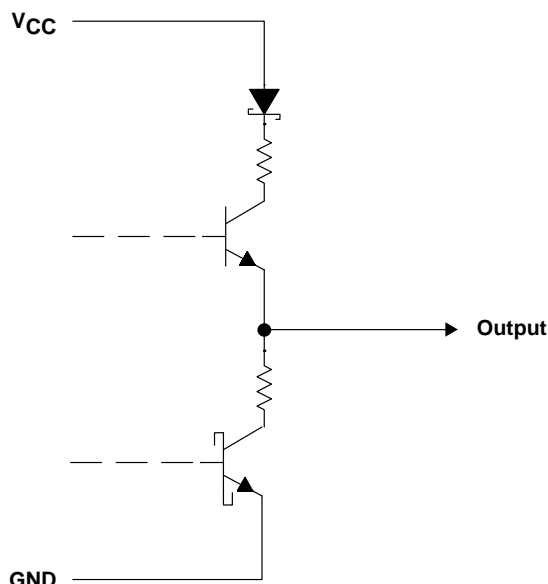
logic diagram (positive logic)



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SCBS106C – JANUARY 1991 – REVISED MARCH 1996

schematic of Y outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O	–0.5 V to 5.5 V
Current into any output in the low state, I_O	30 mA
Input clamp current, I_{IK} ($V_I < 0$)	–18 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2): DB package	0.6 W
DW package	1.6 W
N package	1.3 W
PW package	0.7 W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

SN54ABT2244A, SN74ABT2244A

OCTAL BUFFERS AND LINE/MOS DRIVERS

WITH 3-STATE OUTPUTS

SCBS106C – JANUARY 1991 – REVISED MARCH 1996

recommended operating conditions (see Note 3)

			SN54ABT2244A		SN74ABT2244A		UNIT
			MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V _{IH}	High-level input voltage		2		2		V
V _{IL}	Low-level input voltage			0.8		0.8	V
V _I	Input voltage		0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current			–24		–32	mA
I _{OL}	Low-level output current			12		12	mA
Δt/Δv	Input transition rise or fall rate	Outputs enabled		5		5	ns/V
Δt/ΔV _{CC}	Power-up ramp rate		200		200		μs/V
T _A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T _A = 25°C			SN54ABT2244A		SN74ABT2244A		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V _{IK}	V _{CC} = 4.5 V, I _I = –18 mA				–1.2		–1.2		–1.2	V
V _{OH}	V _{CC} = 4.5 V, I _{OH} = –3 mA		2.5			2.5		2.5		V
	V _{CC} = 5 V, I _{OH} = –3 mA		3			3		3		
	V _{CC} = 4.5 V	I _{OH} = –24 mA	2			2				
		I _{OH} = –32 mA	2*					2		
V _{OL}	V _{CC} = 4.5 V, I _{OL} = 12 mA				0.8		0.8		0.8	V
I _I	V _{CC} = 0 to 5.5 V, V _I = V _{CC} or GND				±1		±1		±1	μA
I _{OZPU}	V _{CC} = 0 to 2.1 V, V _O = 0.5 to 2.7 V, $\overline{OE} = X$				±50				±50	μA
I _{OZPD}	V _{CC} = 2.1 V to 0, V _O = 0.5 to 2.7 V, $\overline{OE} = X$				±50				±50	μA
I _{OZH}	V _{CC} = 2.1 V to 5.5 V, V _O = 2.7 V, $\overline{OE} \geq 2$ V				10		50		10	μA
I _{OZL}	V _{CC} = 2.1 V to 5.5 V, V _O = 0.5 V, $\overline{OE} \geq 2$ V				–10		–50		–10	μA
I _{off}	V _{CC} = 0, V _I or V _O ≤ 4.5 V				±100				±100	μA
I _{CEX}	V _{CC} = 5.5 V, V _O = 5.5 V	Outputs high			50		50		50	μA
I _{O‡}	V _{CC} = 5.5 V, V _O = 2.5 V		–50	–100	–180	–50	–180	–50	–180	mA
I _{CC}	V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND	Outputs high		1	250		250		250	μA
		Outputs low		24	30		30		30	mA
		Outputs disabled		0.5	250		250		250	μA
ΔI _{CC} §	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND	Data inputs								mA
		Outputs enabled			1.5		1.5		1.5	
		Outputs disabled			0.05		0.05		0.05	
	Control inputs				1.5		1.5		1.5	
C _i	V _I = 2.5 V or 0.5 V				4					pF
C _O	V _O = 2.5 V or 0.5 V				5.5					pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at V_{CC} = 5 V.

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.



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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$			SN54ABT2244A		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	A	Y	1	3.4	4.4	1	5.3	ns
t_{PHL}			1	4.5	6.3	1	6.8	
t_{PZH}	\overline{OE}	Y	1.1	3.8	5.5	1.1	6.5	ns
t_{PZL}			2.1	6.3	9	2.1	10.2	
t_{PHZ}	\overline{OE}	Y	2.1	4.5	6.9	2.1	7	ns
t_{PLZ}			1.7	4.3	6.9	1.7	7.4	

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$			SN74ABT2244A		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	A	Y	1	3.4	4.3	1	4.7	ns
t_{PHL}			1	4.5	5.3	1	5.6	
t_{PZH}	\overline{OE}	Y	1.1	3.8	4.8	1.1	5.5	ns
t_{PZL}			2.1	6.3	7.3	2.1	8.3	
t_{PHZ}	\overline{OE}	Y	2.1	4.5	5.6	2.1	6.6	ns
t_{PLZ}			1.7	4.3	5.3	1.7	5.8	

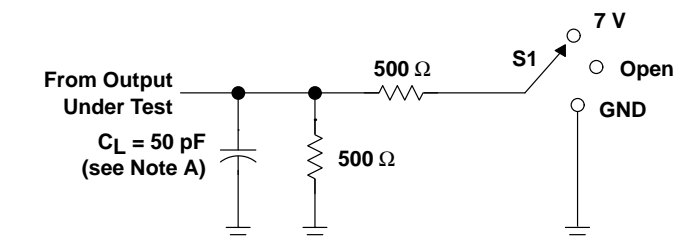
SN54ABT2244A, SN74ABT2244A

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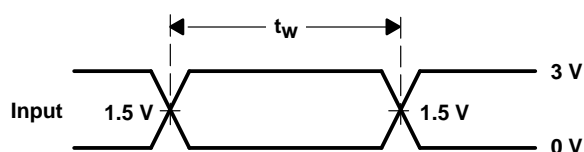
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PARAMETER MEASUREMENT INFORMATION

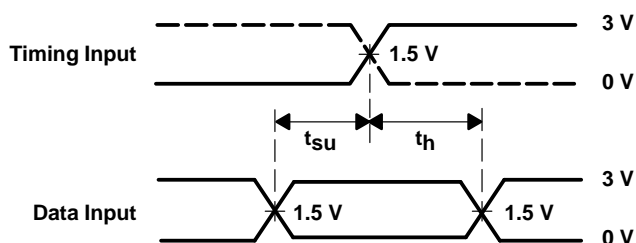


LOAD CIRCUIT FOR OUTPUTS

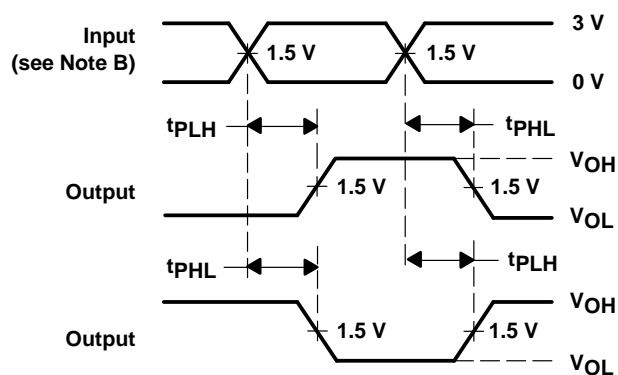
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



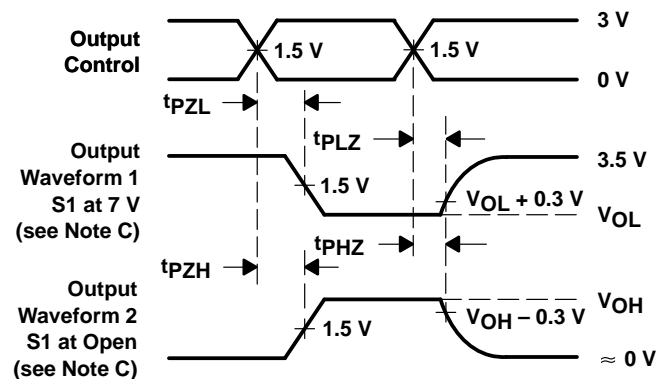
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
- B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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