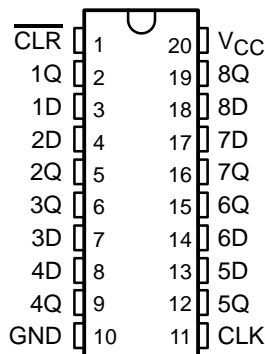


SN54LVT273, SN74LVT273 3.3-V ABT OCTAL D-TYPE FLIP-FLOPS WITH CLEAR

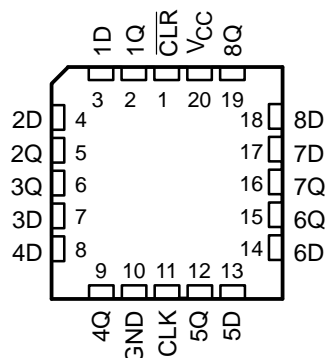
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- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Buffered Clock and Direct Clear Inputs
- Individual Data Input to Each Flip-Flop
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), and Ceramic (J) DIPs

SN54LVT273 . . . J PACKAGE
SN74LVT273 . . . DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVT273 . . . FK PACKAGE
(TOP VIEW)



description

These octal D-type flip-flops are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVT273 are positive-edge-triggered flip-flops with a direct clear input. Information at the data (D) inputs meeting the setup-time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock (CLK) input is at either the high or low level, the D-input signal has no effect at the output.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVT273 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LVT273 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVT273 is characterized for operation from -40°C to 85°C .



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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SN54LVT273, SN74LVT273

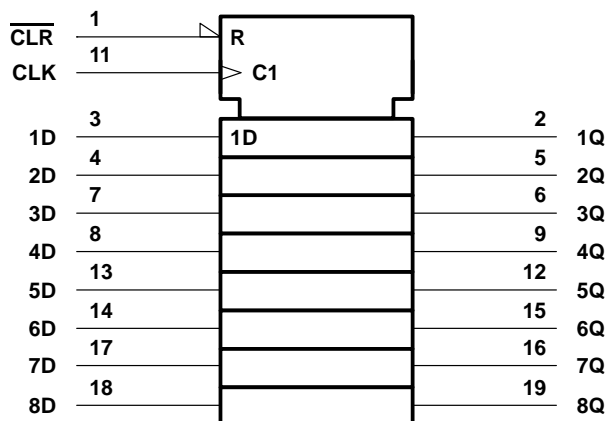
3.3-V ABT OCTAL D-TYPE FLIP-FLOPS WITH CLEAR

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FUNCTION TABLE
(each flip-flop)

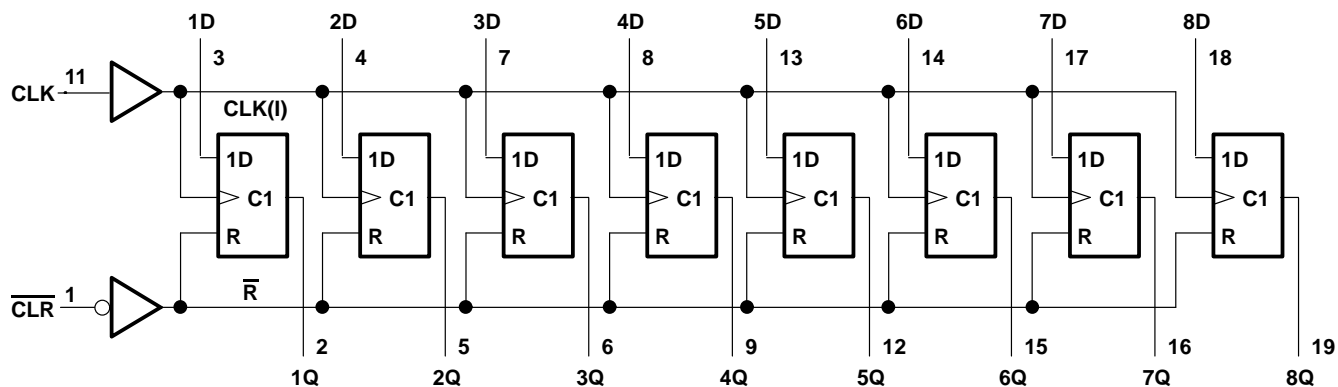
INPUTS			OUTPUT Q
$\overline{\text{CLR}}$	CLK	D	
L	X	X	L
H	\uparrow	H	H
H	\uparrow	L	L
H	H or L	X	Q_0

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SN54LVT273, SN74LVT273 3.3-V ABT OCTAL D-TYPE FLIP-FLOPS WITH CLEAR

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Current into any output in the low state, I_O : SN54LVT273	96 mA
SN74LVT273	128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT273	48 mA
SN74LVT273	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 3): DB package	0.6 W
DW package	1.6 W
PW package	0.7 W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 4)

		SN54LVT273		SN74LVT273		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage		5.5		5.5	V
I_{OH}	High-level output current		–24		–32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		10		10	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

SN54LVT273, SN74LVT273

3.3-V ABT OCTAL D-TYPE FLIP-FLOPS

WITH CLEAR

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN54LVT273			SN74LVT273			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{IK}	V _{CC} = 2.7 V, I _I = −18 mA			−1.2			−1.2			V
V _{OH}	V _{CC} = MIN to MAX‡, I _{OH} = −100 μA			V _{CC} − 0.2			V _{CC} − 0.2			V
	V _{CC} = 2.7 V, I _{OH} = − 8 mA			2.4			2.4			
	V _{CC} = 3 V	I _{OH} = − 24 mA		2						
		I _{OH} = −32 mA					2			
V _{OL}	V _{CC} = 2.7 V	I _{OL} = 100 μA		0.2			0.2			V
		I _{OL} = 24 mA		0.5			0.5			
	V _{CC} = 3 V	I _{OL} = 16 mA		0.4			0.4			
		I _{OL} = 32 mA		0.5			0.5			
		I _{OL} = 48 mA		0.55						
		I _{OL} = 64 mA					0.55			
		I _I	V _{CC} = 0 or MAX‡, V _I = 5.5 V		10			10		
V _{CC} = 3.6 V	V _I = V _{CC} or GND		Control inputs	±1			±1			
	V _I = V _{CC}		Data inputs	1			1			
	V _I = 0			−5			−5			
I _I (hold)	V _{CC} = 3 V	V _I = 0.8 V	Data inputs	75			75			μA
		V _I = 2 V		−75			−75			
I _{CC}	V _{CC} = 3.6 V, V _I = V _{CC} or GND, I _O = 0,		Outputs high	0.12	0.19	0.12		0.19	mA	
			Outputs low	8.6	12	8.6		12		
ΔI _{CC} §	V _{CC} = 3 V to 3.6 V, One input at V _{CC} − 0.6 V, Other inputs at V _{CC} or GND			0.2			0.2			mA
C _i	V _I = 3 V or 0						4			pF
C _o	V _O = 3 V or 0						8			pF

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		SN54LVT273				SN74LVT273				UNIT
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency					0	150			MHz
t_w	Pulse duration					3.3		3.3		ns
t_{su}	Setup time, data high or low before CLK↑					2.3		2.7		ns
	Setup time, $\overline{\text{CLR}}$ high before CLK↑					2.7		3.2		
t_h	Hold time, data high or low after CLK↑					0		0		ns

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switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT273				SN74LVT273				UNIT	
			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN		MAX
f _{max}							150				MHz	
t _{PLH}	CLK	Any Q					1.7	3.5	5.5	6.3	ns	
t _{PHL}							1.9	3.5	5.5	5.9		
t _{PHL}	$\overline{\text{CLR}}$	Any Q					1.3	3.2	5.1	6.2	ns	

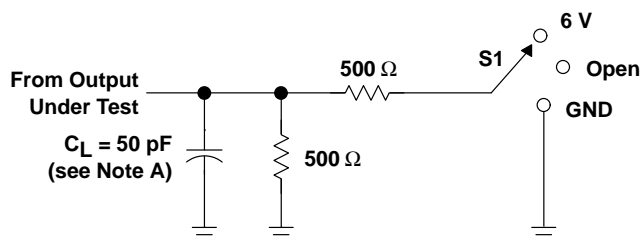
† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

SN54LVT273, SN74LVT273

3.3-V ABT OCTAL D-TYPE FLIP-FLOPS WITH CLEAR

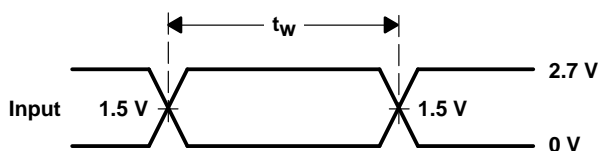
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PARAMETER MEASUREMENT INFORMATION

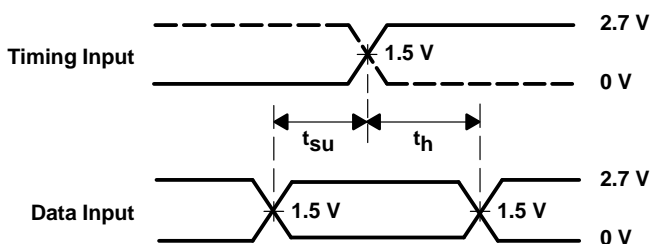


LOAD CIRCUIT FOR OUTPUTS

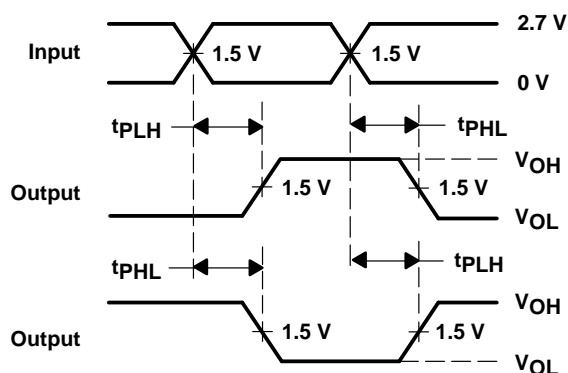
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



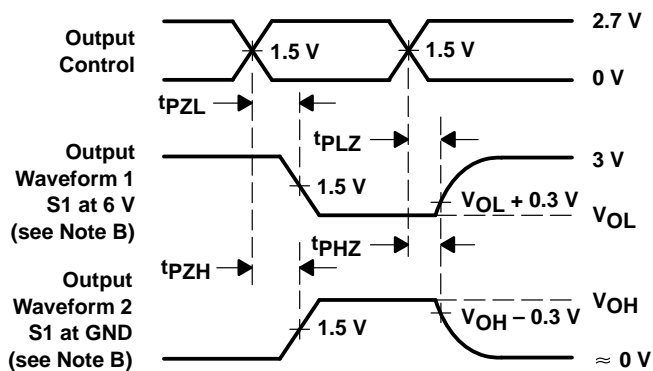
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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