

SN54LVT543, SN74LVT543 3.3-V ABT OCTAL REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS137D – MAY 1992 – REVISED JULY 1995

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Support Live Insertion
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), and Ceramic (JT) DIPs

description

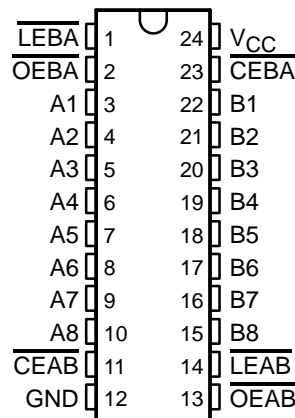
These octal transceivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVT543 contain two sets of D-type latches for temporary storage of data flowing in either direction. Separate latch-enable (\overline{LEAB} or \overline{LEBA}) and output-enable (\overline{OEAB} or \overline{OEBA}) inputs are provided for each register to permit independent control in either direction of data flow.

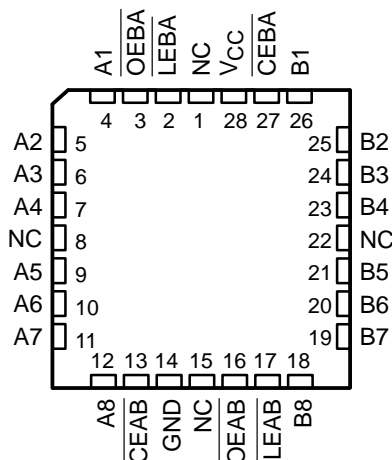
The A-to-B enable (\overline{CEAB}) input must be low in order to enter data from A or to output data from B. If \overline{CEAB} is low and \overline{LEAB} is low, the A-to-B latches are transparent; a subsequent low-to-high transition of \overline{LEAB} puts the A latches in the storage mode. With \overline{CEAB} and \overline{OEAB} both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar but requires using the \overline{CEBA} , \overline{LEBA} , and \overline{OEBA} inputs.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

SN54LVT543 . . . JT PACKAGE
SN74LVT543 . . . DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVT543 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection



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description (continued)

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVT543 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

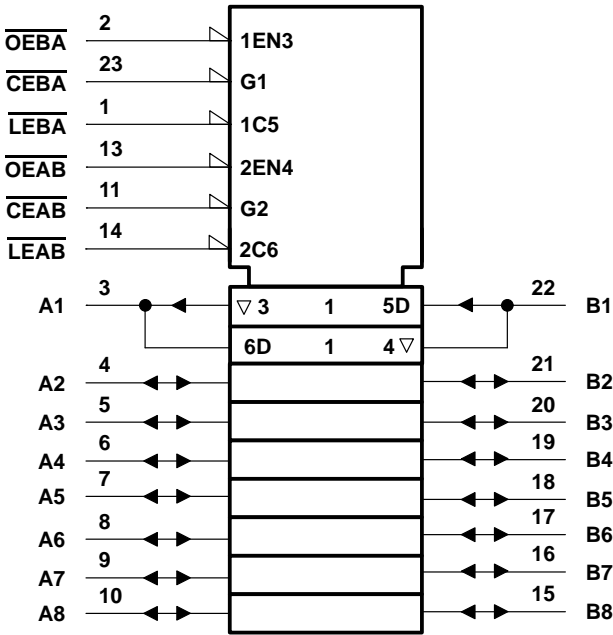
The SN54LVT543 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVT543 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE†				
INPUTS				OUTPUT B
\overline{CEAB}	\overline{LEAB}	\overline{OEAB}	A	
H	X	X	X	Z
X	X	H	X	Z
L	H	L	X	B_0^{\ddagger}
L	L	L	L	L
L	L	L	H	H

† A-to-B data flow is shown; B-to-A flow control is the same except that it uses \overline{CEBA} , \overline{LEBA} , and \overline{OEBA} .

‡ Output level before the indicated steady-state input conditions were established

logic symbol§



§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DB, DW, JT, and PW packages.

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The diagram illustrates the logic for the B1 channel receiver. It features four 2-input AND gates at the input, each with one input from a data line (OEBA, CEBA, LEBA, OEAB) and one from a common clock line (23). The outputs of these AND gates are connected to a network of inverters, D-type flip-flops (C1 1D), and multiplexers. The final output is B1 (22). A feedback loop connects B1 back to the input of the first AND gate via a multiplexer. The diagram also shows connections to other channels.

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recommended operating conditions (see Note 4)

			SN54LVT543		SN74LVT543		UNIT
			MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V _{IH}	High-level input voltage		2		2		V
V _{IL}	Low-level input voltage			0.8		0.8	V
V _I	Input voltage			5.5		5.5	V
I _{OH}	High-level output current			–24		–32	mA
I _{OL}	Low-level output current			48		64	mA
Δt/Δv	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T _A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54LVT543			SN74LVT543			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	$V_{CC} = 2.7\text{ V}$, $I_I = -18\text{ mA}$				-1.2			-1.2	V
V_{OH}	$V_{CC} = \text{MIN to MAX}^\ddagger$, $I_{OH} = -100\text{ }\mu\text{A}$		$V_{CC}-0.2$			$V_{CC}-0.2$			V
	$V_{CC} = 2.7\text{ V}$, $I_{OH} = -8\text{ mA}$		2.4			2.4			
	$V_{CC} = 3\text{ V}$	$I_{OH} = -24\text{ mA}$	2						
		$I_{OH} = -32\text{ mA}$				2			
V_{OL}	$V_{CC} = 2.7\text{ V}$	$I_{OL} = 100\text{ }\mu\text{A}$			0.2			0.2	V
		$I_{OL} = 24\text{ mA}$			0.5			0.5	
	$V_{CC} = 3\text{ V}$	$I_{OL} = 16\text{ mA}$			0.4			0.4	
		$I_{OL} = 32\text{ mA}$			0.5			0.5	
		$I_{OL} = 48\text{ mA}$			0.55				
		$I_{OL} = 64\text{ mA}$						0.55	
I_I	$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}\text{ or GND}$	Control inputs			± 1			± 1	μA
	$V_{CC} = 0\text{ or MAX}^\ddagger$, $V_I = 5.5\text{ V}$				10			10	
	$V_{CC} = 3.6\text{ V}$	$V_I = 5.5\text{ V}$			20			20	
		$V_I = V_{CC}$			5			5	
		$V_I = 0$			-10			-10	
I_{off}	$V_{CC} = 0$, $V_I\text{ or }V_O = 0\text{ to }4.5\text{ V}$							± 100	μA
$I_{I(\text{hold})}$	$V_{CC} = 3\text{ V}$	$V_I = 0.8\text{ V}$	A or B ports		75			75	μA
		$V_I = 2\text{ V}$			-75			-75	
I_{OZH}	$V_{CC} = 3.6\text{ V}$, $V_O = 3\text{ V}$				1			1	μA
I_{OZL}	$V_{CC} = 3.6\text{ V}$, $V_O = 0.5\text{ V}$				-1			-1	μA
I_{CC}	$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}\text{ or GND}$, $I_O = 0$	Outputs high		0.13	0.19		0.13	0.19	mA
		Outputs low		8.8	12		8.8	12	
		Outputs disabled		0.13	0.19		0.13	0.19	
ΔI_{CC}^\P	$V_{CC} = 3\text{ V to }3.6\text{ V}$, One input at $V_{CC} - 0.6\text{ V}$, Other inputs at $V_{CC}\text{ or GND}$				0.2			0.2	mA
C_i	$V_I = 3\text{ V or }0$				4.5			4.5	pF
C_{io}	$V_O = 3\text{ V or }0$				11			11	pF

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

§ Unused terminals at V_{CC} or GND

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

				SN54LVT543				SN74LVT543				UNIT
				$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, \overline{LEAB} or \overline{LEBA} low			3.3		3.3		3.3		3.3		ns
t_{su}	Setup time	A or B before \overline{LEAB} or $\overline{LEBA}\uparrow$		Data high	0		0		0		0	ns
				Data low	0.8		1.1		0.8		1.1	
		A or B before \overline{CEAB} or $\overline{CEBA}\uparrow$		Data high	0		0		0		0	
				Data low	0.9		1.2		0.9		1.2	
t_h	Hold time	A or B after \overline{LEAB} or $\overline{LEBA}\uparrow$			1.7		1.7		1.7		1.7	ns
		A or B after \overline{CEAB} or $\overline{CEBA}\uparrow$			1.8		1.8		1.8		1.8	

switching characteristics over recommended operating free-air temperature range, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

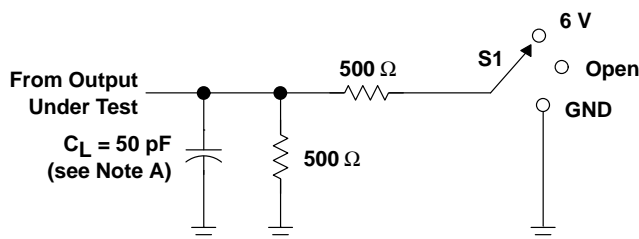
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT543				SN74LVT543				UNIT	
			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V			
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN		MAX
t _{PLH}	A or B	B or A	1	4.9	5.7		1	2.9	4.7	5.5		ns
t _{PHL}			1	4.8	6		1	3.3	4.6	5.8		
t _{PLH}	\overline{LE}	A or B	1	6.1	7.5		1	4	5.9	7.3		ns
t _{PHL}			1	5.9	7.5		1	4.1	5.7	7.3		
t _{PZH}	\overline{OE}	A or B	1	6	7.8		1	4.1	5.8	7.6		ns
t _{PZL}			1.1	6.6	8.4		1.1	4.5	6.4	8.2		
t _{PHZ}	\overline{OE}	A or B	2.4	6.7	7.3		2.4	4.8	6.5	7.1		ns
t _{PLZ}			2	6	6.1		2	4	5.8	5.9		
t _{PZH}	\overline{CE}	A or B	1	6.2	7.8		1	4.2	6	7.6		ns
t _{PZL}			1.4	6.9	8.5		1.4	4.7	6.7	8.3		
t _{PHZ}	\overline{CE}	A or B	2.3	6.6	7.3		2.3	4.7	6.4	7.1		ns
t _{PLZ}			2	5.6	5.8		2	3.8	5.4	5.6		

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

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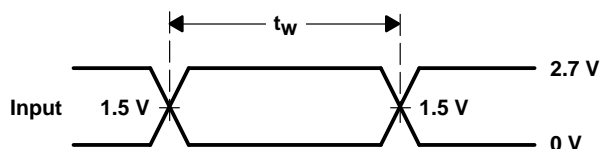
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PARAMETER MEASUREMENT INFORMATION

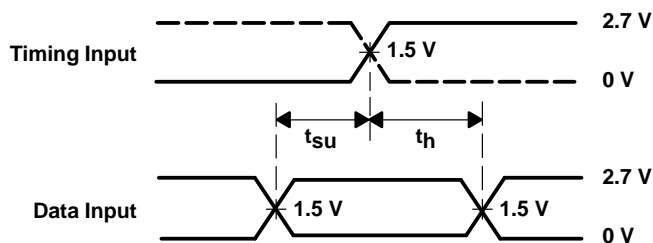


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

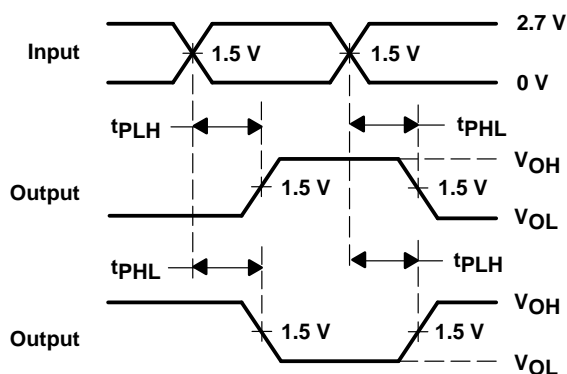
LOAD CIRCUIT FOR OUTPUTS



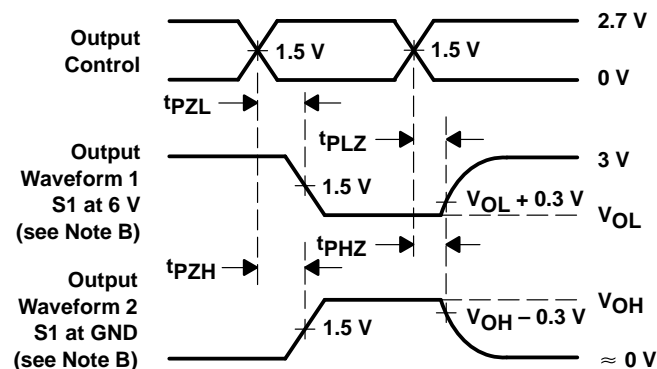
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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