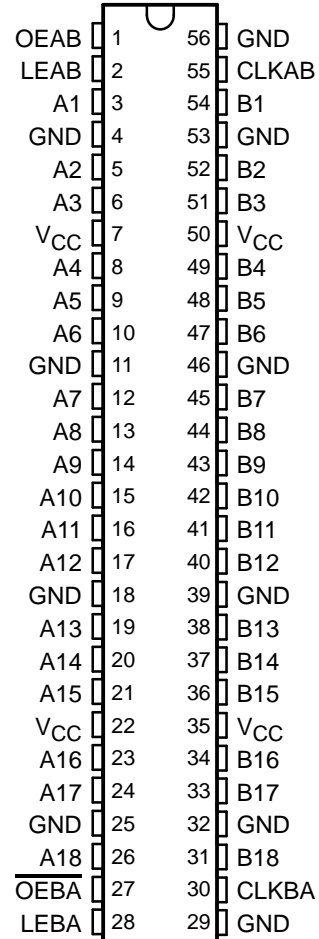


# SN54LVT16501, SN74LVT16501 3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS147F – MAY 1992 – REVISED MAY 1996

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Members of the Texas Instruments *Widebus*™ Family
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V  $V_{CC}$ )
- Support Unregulated Battery Operation Down to 2.7 V
- *UBT*™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode
- Typical  $V_{OLP}$  (Output Ground Bounce)  $< 0.8$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model ( $C = 200$  pF,  $R = 0$ )
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Support Live Insertion
- Distributed  $V_{CC}$  and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

SN54LVT16501 ... WD PACKAGE  
SN74LVT16501 ... DGG OR DL PACKAGE  
(TOP VIEW)



## description

The 'LVT16501 are 18-bit universal bus transceivers designed for low-voltage (3.3-V)  $V_{CC}$  operation, but with the capability to provide a TTL interface to a 5-V system environment.

Data flow in each direction is controlled by output-enable (OEAB and  $\overline{OEBA}$ ), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the devices operate in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. When OEAB is high, the outputs are active. When OEAB is low, the outputs are in the high-impedance state.



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# SN54LVT16501, SN74LVT16501

## 3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS

### WITH 3-STATE OUTPUTS

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#### description (continued)

Data flow for B to A is similar to that of A to B but uses  $\overline{OEBA}$ , LEBA, and CLKBA. The output enables are complementary (OEAB is active high and  $\overline{OEBA}$  is active low).

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor. The minimum value of the resistor is determined by the current-sinking capability of the driver. OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The SN74LVT16501 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the input/output (I/O) pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVT16501 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74LVT16501 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

FUNCTION TABLE†				
INPUTS				OUTPUT B
OEAB	LEAB	CLKAB	A	
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↑	L	L
H	L	↑	H	H
H	L	H	X	B <sub>0</sub> ‡
H	L	L	X	B <sub>0</sub> §

† A-to-B data flow is shown; B-to-A flow is similar but uses  $\overline{OEBA}$ , LEBA, and CLKBA.

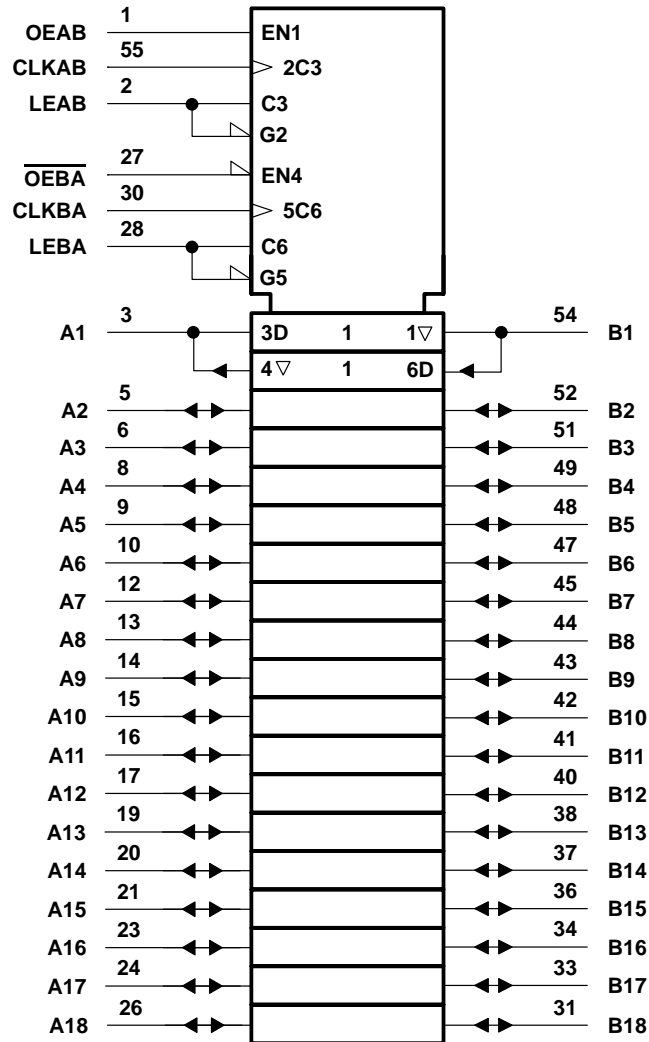
‡ Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low

§ Output level before the indicated steady-state input conditions were established

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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

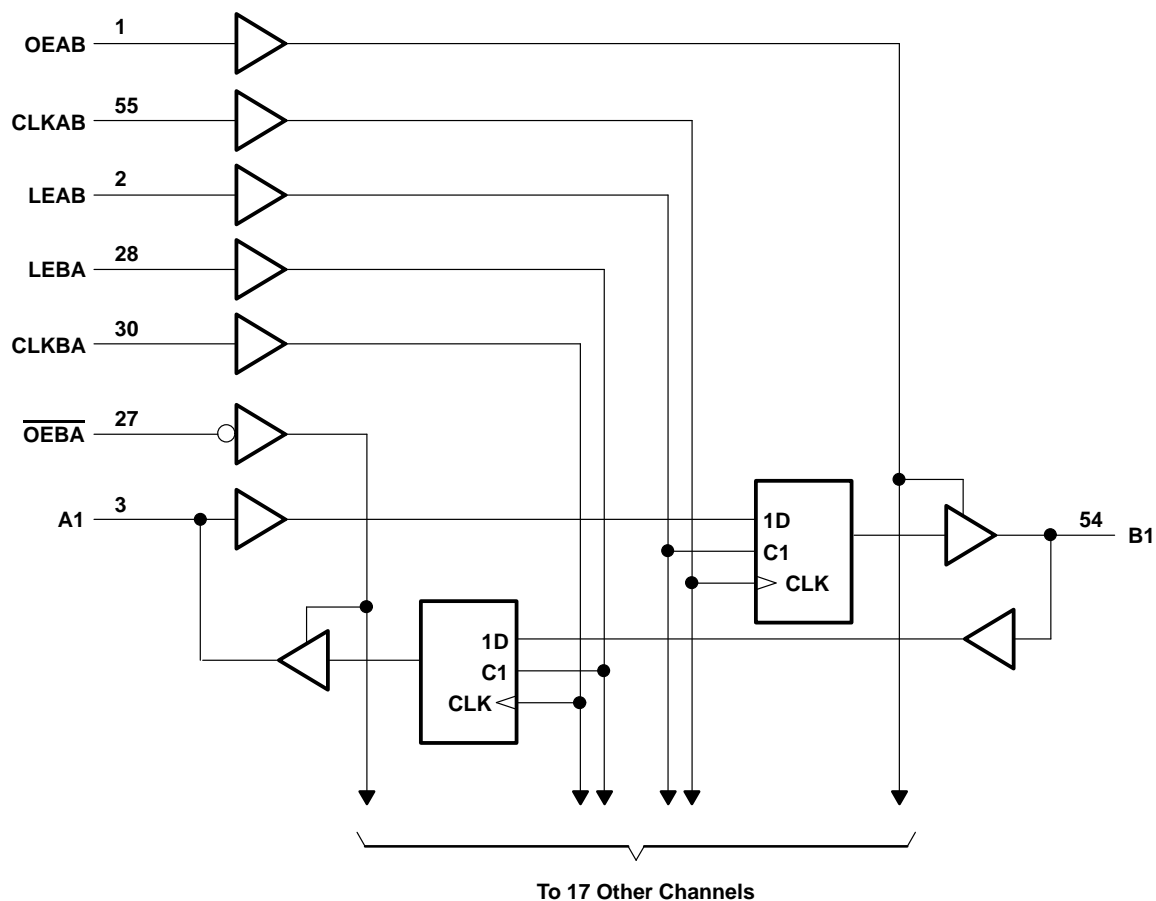
# SN54LVT16501, SN74LVT16501

## 3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS

### WITH 3-STATE OUTPUTS

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#### logic diagram (positive logic)



# SN54LVT16501, SN74LVT16501

## 3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS

### WITH 3-STATE OUTPUTS

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#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	–0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, $V_O$ (see Note 1)	–0.5 V to 7 V
Current into any output in the low state, $I_O$ : SN54LVT16501	96 mA
SN74LVT16501	128 mA
Current into any output in the high state, $I_O$ (see Note 2): SN54LVT16501	48 mA
SN74LVT16501	64 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ )	–50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 3): DGG package	1 W
DL package	1.4 W
Operating free-air temperature range, $T_A$ : SN54LVT16501	–55°C to 125°C
SN74LVT16501	–40°C to 85°C
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
  2. This current flows only when the output is in the high state and  $V_O > V_{CC}$ .
  3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*.

#### recommended operating conditions (see Note 4)

		SN54LVT16501		SN74LVT16501		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	2.7	3.6	2.7	3.6	V
$V_{IH}$	High-level input voltage	2		2		V
$V_{IL}$	Low-level input voltage		0.8		0.8	V
$V_I$	Input voltage		5.5		5.5	V
$I_{OH}$	High-level output current		–24		–32	mA
$I_{OL}$	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	ns/V
$T_A$	Operating free-air temperature	–55	125	–40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.



# SN54LVT16501, SN74LVT16501

## 3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS

### WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54LVT16501			SN74LVT16501			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
$V_{IK}$		$V_{CC} = 2.7\text{ V}$ , $I_I = -18\text{ mA}$			-1.2			-1.2	V
$V_{OH}$		$V_{CC} = \text{MIN to MAX}^\ddagger$ , $I_{OH} = -100\text{ }\mu\text{A}$	$V_{CC}-0.2$			$V_{CC}-0.2$			V
		$V_{CC} = 2.7\text{ V}$ , $I_{OH} = -8\text{ mA}$	2.4			2.4			
	$V_{CC} = 3\text{ V}$	$I_{OH} = -24\text{ mA}$	2						
		$I_{OH} = -32\text{ mA}$				2			
$V_{OL}$	$V_{CC} = 2.7\text{ V}$	$I_{OL} = 100\text{ }\mu\text{A}$			0.2			0.2	V
		$I_{OL} = 24\text{ mA}$			0.5			0.5	
	$V_{CC} = 3\text{ V}$	$I_{OL} = 16\text{ mA}$			0.4			0.4	
		$I_{OL} = 32\text{ mA}$			0.5			0.5	
		$I_{OL} = 48\text{ mA}$			0.55				
		$I_{OL} = 64\text{ mA}$						0.55	
$I_I$	Control pins	$V_{CC} = 3.6\text{ V}$ , $V_I = V_{CC}\text{ or GND}$			$\pm 1$			$\pm 1$	$\mu\text{A}$
		$V_{CC} = 0\text{ or MAX}^\ddagger$ , $V_I = 5.5\text{ V}$			10			10	
	A or B ports§	$V_{CC} = 3.6\text{ V}$ , $V_I = 5.5\text{ V}$			120			20	
		$V_I = V_{CC}$			1			1	
		$V_I = 0$			-5			-5	
$I_{off}$		$V_{CC} = 0$ , $V_I\text{ or }V_O = 0\text{ to }4.5\text{ V}$						$\pm 100$	$\mu\text{A}$
$I_I(\text{hold})$	A or B ports	$V_{CC} = 3\text{ V}$ , $V_I = 0.8\text{ V}$		75			75		$\mu\text{A}$
		$V_I = 2\text{ V}$		-75			-75		
$I_{OZH}$		$V_{CC} = 3.6\text{ V}$ , $V_O = 3\text{ V}$						1	$\mu\text{A}$
$I_{OZL}$		$V_{CC} = 3.6\text{ V}$ , $V_O = 0.5\text{ V}$						-1	$\mu\text{A}$
$I_{CC}$	$V_{CC} = 3.6\text{ V}$ , $V_I = V_{CC}\text{ or GND}$	$I_O = 0$ , Outputs high			0.12			0.12	mA
					5			5	
					0.12			0.12	
$\Delta I_{CC}^\parallel$		$V_{CC} = 3\text{ V to }3.6\text{ V}$ , One input at $V_{CC} - 0.6\text{ V}$ , Other inputs at $V_{CC}\text{ or GND}$			0.2			0.2	mA
$C_i$		$V_I = 3\text{ V or }0$		3.5			3.5		pF
$C_{io}$		$V_O = 3\text{ V or }0$		12			12		pF

† All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

§ Unused pins at  $V_{CC}$  or GND

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND.

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**WITH 3-STATE OUTPUTS**

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**timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)**

			SN54LVT16501				SN74LVT16501				UNIT
			$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$f_{\text{clock}}$	Clock frequency		0	150	0	125	0	150	0	125	MHz
$t_w$	Pulse duration	LE high	3.3		3.3		3.3		3.3		ns
		CLK high or low	3.3		3.3		3.3		3.3		
$t_{\text{su}}$	Setup time	A before CLKAB↑	1.6		2.1		1.6		2.1		ns
		B before CLKBA↑	1.6		2.1		1.6		2.1		
		A or B before LE↓, $\overline{\text{CLK}}$ high	3.1		2.7		2.6		1.9		
		A or B before LE↓, $\overline{\text{CLK}}$ low	2.6		2.0		2		1.3		
$t_h$	Hold time	A or B after CLK↑	2		2.1		2		2.1		ns
		A or B after LE↓	1.3		1.2		0.9		1.2		

**switching characteristics over recommended operating free-air temperature range,  $C_L = 50\text{ pF}$  (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT16501				SN74LVT16501				UNIT	
			V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V			V <sub>CC</sub> = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN		MAX
f <sub>max</sub>			150		125		150		125		MHz	
t <sub>PLH</sub>	B or A	A or B	1.7	5.4	6.8	1.7	3	5.4	6.8	ns		
t <sub>PHL</sub>			1.6	6	7.8	1.6	3.2	5.9	7.7			
t <sub>PLH</sub>	LEBA or LEAB	A or B	2.3	7.3	9	2.3	4	7	8.5	ns		
t <sub>PHL</sub>			2.7	8.2	9.8	2.7	4.3	7.9	9.7			
t <sub>PLH</sub>	CLKBA or CLKAB	A or B	2.5	8.3	9.7	2.5	4.1	7.9	9.2	ns		
t <sub>PHL</sub>			3.5	9.4	10.7	3.5	5.4	8.9	10.4			
t <sub>PZH</sub>	$\overline{\text{OEBA}}$ or OEAB	A or B	1.2	5.1	6.1	1.2	3	5	5.9	ns		
t <sub>PZL</sub>			1.5	5.9	7	1.5	3	5.8	6.9			
t <sub>PHZ</sub>	$\overline{\text{OEBA}}$ or OEAB	A or B	2.7	7.5	8.5	2.7	4.6	7.4	8.3	ns		
t <sub>PLZ</sub>			2.8	6.8	7.5	2.8	4.7	6.7	7.2			

$\dagger$  All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

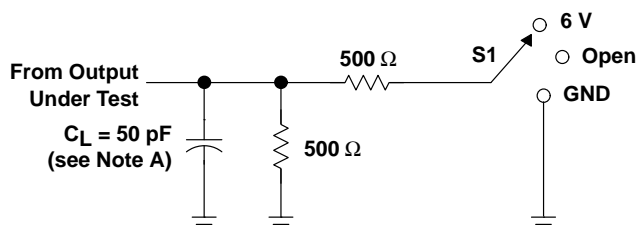
# SN54LVT16501, SN74LVT16501

## 3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS

### WITH 3-STATE OUTPUTS

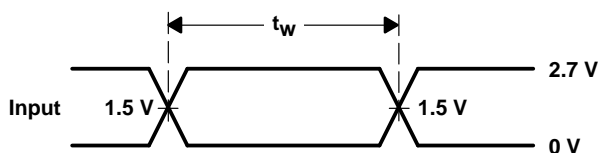
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#### PARAMETER MEASUREMENT INFORMATION

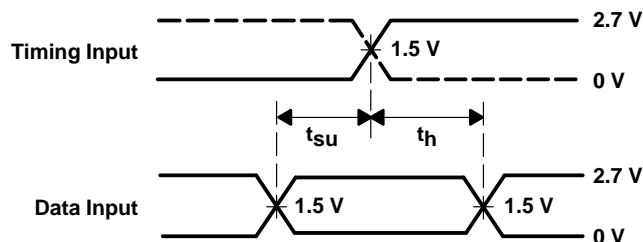


LOAD CIRCUIT

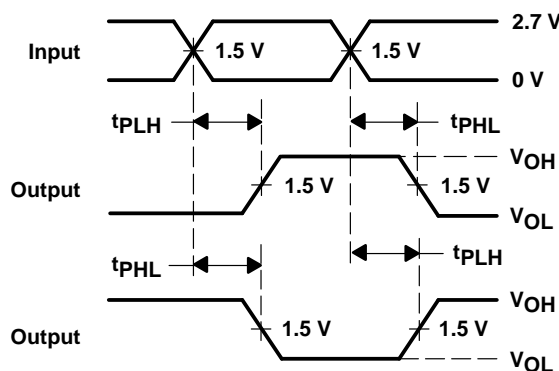
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND



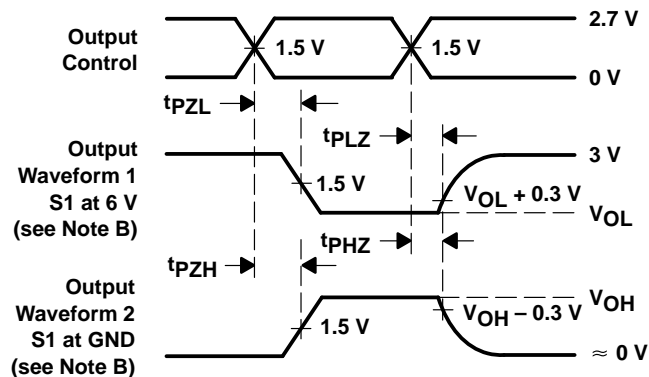
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



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