

SN54ABT377, SN74ABT377A OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH CLOCK ENABLE

SCBS156D – FEBRUARY 1991 – REVISED JULY 1996

- State-of-the-Art **EPIC-II^B**™ BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce) < 1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- High-Drive Outputs (–32-mA I_{OH} , 64-mA I_{OL})
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Package Options Include Plastic Small-Outline (DW) and Shrink Small-Outline (DB) Packages, Ceramic Chip Carriers (FK), and Plastic (N) and Ceramic (J) DIPs, and Ceramic Flat (W) Packages

description

These 8-bit positive-edge-triggered D-type flip-flops with a clock (CLK) input are particularly suitable for implementing buffer and storage registers, shift registers, and pattern generators.

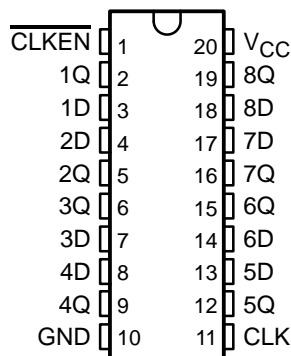
Data (D) input information that meets the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse if the common clock-enable ($\overline{\text{CLKEN}}$) input is low.

Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the buffered clock (CLK) input is at either the high or low level, the D input signal has no effect at the output. The circuits are designed to prevent false clocking by transitions at $\overline{\text{CLKEN}}$.

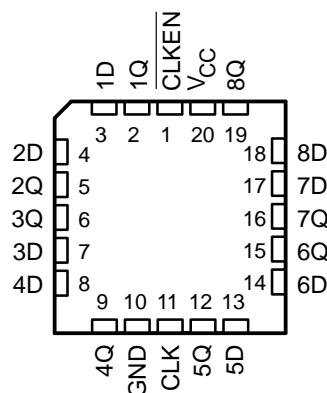
The SN74ABT377A is available in TI's shrink small-outline package, which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54ABT377 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ABT377A is characterized for operation from -40°C to 85°C .

SN54ABT377 . . . J OR W PACKAGE
SN74ABT377A . . . DB, DW, OR N PACKAGE
(TOP VIEW)



SN54ABT377 . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT Q
$\overline{\text{CLKEN}}$	CLK	D	
H	X	X	Q_0
L	↑	H	H
L	↑	L	L
X	H or L	X	Q_0



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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The logic diagram shows a 1-bit counter implemented with a D flip-flop. The inputs are CLK (11), CLKEN (1), and 1D (3). The output is 1Q (2). The circuit includes an inverter, two AND gates, an OR gate, and a D flip-flop. The output of the flip-flop is 1Q (2). The circuit is connected to seven other channels, as indicated by the bracketed lines at the bottom.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O	–0.5 V to 5.5 V
Current into any output in the low state, I_O : SN54ABT377	96 mA
SN74ABT377A	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	–18 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2): DB package	0.6 W
DW package	1.6 W
N package	1.3 W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*.

recommended operating conditions (see Note 3)

	SN54ABT377		SN74ABT377A		UNIT
	MIN	MAX	MIN	MAX	
V_{CC} Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH} High-level input voltage	2		2		V
V_{IL} Low-level input voltage		0.8		0.8	V
V_I Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH} High-level output current		–24		–32	mA
I_{OL} Low-level output current		48		64	mA
$\Delta t/\Delta v$ Input transition rise or fall rate		5		5	ns/V
T_A Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T _A = 25°C			SN54ABT377		SN74ABT377A		UNIT
		MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA			-1.2		-1.2		-1.2	V
V _{OH}	V _{CC} = 4.5 V, I _{OH} = -3 mA	2.5			2.5		2.5		V
	V _{CC} = 5 V, I _{OH} = -3 mA	3			3		3		
	V _{CC} = 4.5 V	I _{OH} = -24 mA	2		2				
		I _{OH} = -32 mA	2*				2		
V _{OL}	V _{CC} = 4.5 V	I _{OL} = 48 mA		0.55		0.55			V
		I _{OL} = 64 mA		0.55*				0.55	
I _I	V _{CC} = 5.5 V, V _I = V _{CC} or GND			±1		±1		±1	μA
I _{off}	V _{CC} = 0, V _I or V _O ≤ 4.5 V			±100				±100	μA
I _{CEX}	V _{CC} = 5.5 V, V _O = 5.5 V	Outputs high		50		50		50	μA
I _{O‡}	V _{CC} = 5.5 V, V _O = 2.5 V			-50 -100 -180		-50 -180		-50 -180	mA
I _{CC}	V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND	Outputs high		1 250		250		250	μA
		Outputs low		24 30		30		30	mA
ΔI _{CC} §	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND			1.5		1.5		1.5	mA
C _i	V _I = 2.5 V or 0.5 V			3.5					pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at V_{CC} = 5 V.

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			V _{CC} = 5 V, T _A = 25°C		SN54ABT377		UNIT
			MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency		0	150	0	150	MHz
t _w	Pulse duration	CLK high or low	3.3		3.3		ns
t _{su}	Setup time before CLK↑	Data high or low	2		2.5		ns
		CLKEN high or low	3		3		
t _h	Hold time after CLK↑	Data high or low	1.8¶		1.8¶		ns
		CLKEN high or low	1.8¶		1.8¶		

¶ This data sheet limit may vary among suppliers.



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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			V _{CC} = 5 V, T _A = 25°C		SN74ABT377A		UNIT
			MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency		0	150	0	150	MHz
t _w	Pulse duration	CLK high or low	3.3		3.3		ns
t _{su}	Setup time before CLK↑	Data high or low	2		2		ns
		CLKEN high or low	3		3		
t _h	Hold time after CLK↑	Data high or low	1.8†		1.8†		ns
		CLKEN high or low	1.2†		1.2†		

† This data sheet limit may vary among suppliers.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, T _A = 25°C			SN54ABT377		UNIT
			MIN	TYP	MAX	MIN	MAX	
f _{max}			150			150		MHz
t _{PLH}	CLK	Q	2.2	4.5	6	2.2	7	ns
t _{PHL}			3.1	5.3	6.8	2	7.6	

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, T _A = 25°C			SN74ABT377A		UNIT
			MIN	TYP	MAX	MIN	MAX	
f _{max}			150			150		MHz
t _{PLH}	CLK	Q	2.2	4.5	6	2.2	6.5	ns
t _{PHL}			2.6†	5.3	6.8	2.6†	7.3	

† This data sheet limit may vary among suppliers.

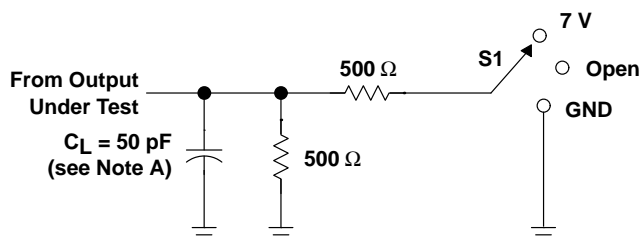
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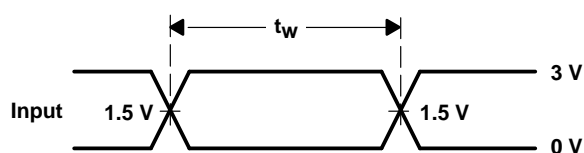
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PARAMETER MEASUREMENT INFORMATION

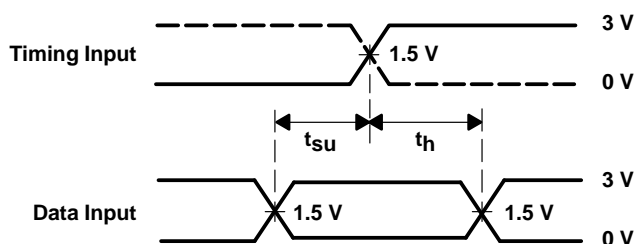


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

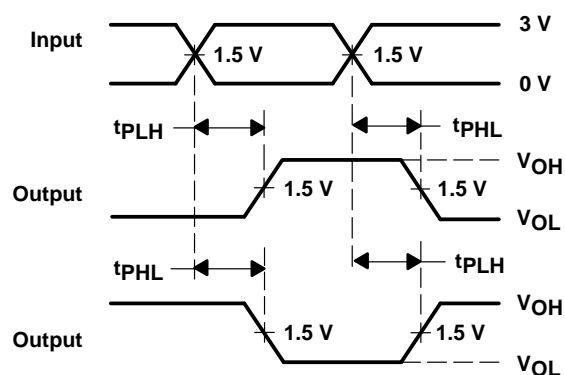
LOAD CIRCUIT



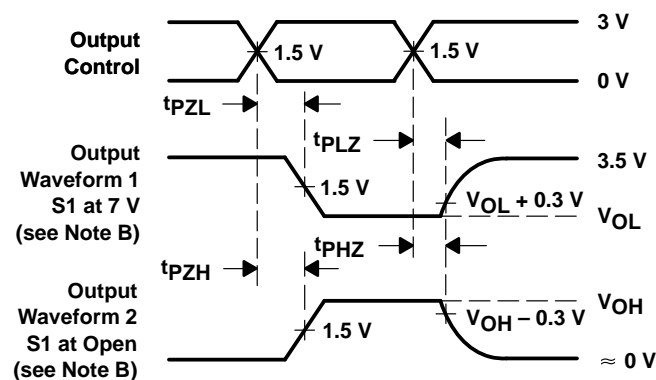
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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