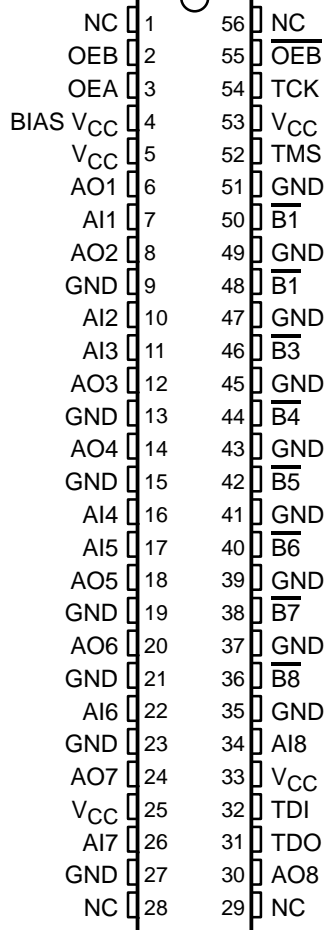


SN54FB2040, SN74FB2040 8-BIT TTL/BTL TRANSCEIVERS

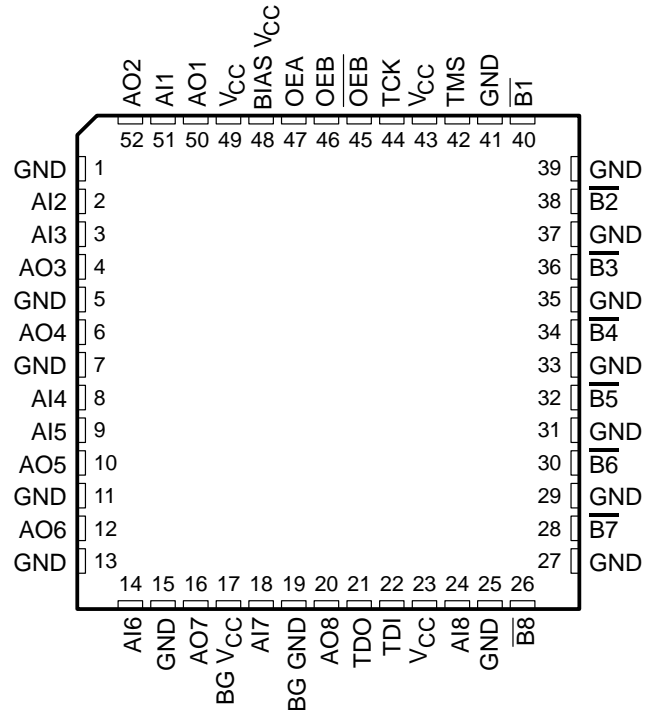
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- Compatible With IEEE 1194.1-1991 (BTL) Standard
- TTL A Port, Backplane Transceiver Logic (BTL) \bar{B} Port
- Open-Collector \bar{B} -Port Outputs Sink 100 mA
- Isolated Logic-Ground and Bus-Ground Pins Reduce Noise
- BIAS V_{CC} Pin Minimizes Signal Distortion During Live Insertion/Withdrawal
- \bar{B} -Port Biasing Network Preconditions the Connector and PC Trace to the BTL High-Level Voltage
- Package Options Include Plastic Quad Flat (RC) Package and Ceramic Flat (WD) Package

SN54FB2040 . . . WD PACKAGE
(TOP VIEW)



SN74FB2040 . . . RC PACKAGE
(TOP VIEW)



NC – No internal connection



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SN54FB2040, SN74FB2040

8-BIT TTL/BTL TRANSCEIVERS

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description

The 'FB2040 are 8-bit transceivers designed to translate signals between TTL and backplane transceiver logic (BTL) environments.

The \overline{B} port operates at BTL-signal levels. The open-collector \overline{B} ports are specified to sink 100 mA. Two output enables, OEB and \overline{OEB} , are provided for the \overline{B} outputs. When OEB is high and \overline{OEB} is low, the \overline{B} port is active and reflects the inverse of the data present at the A-input pins. When OEB is low, \overline{OEB} is high, or V_{CC} is typically less than 2.5 V, the \overline{B} port is turned off.

The A port operates at TTL-signal levels and has split input and output pins. The A outputs reflect the inverse of the data at the \overline{B} port when the A-port output enable, OEA, is high. When OEA is low or when V_{CC} is typically less than 2.5 V, the A outputs are in the high-impedance state.

Pins are allocated for the four-wire IEEE 1149.1 (JTAG) test bus. Currently, TMS and TCK are not connected and TDI is shorted to TDO.

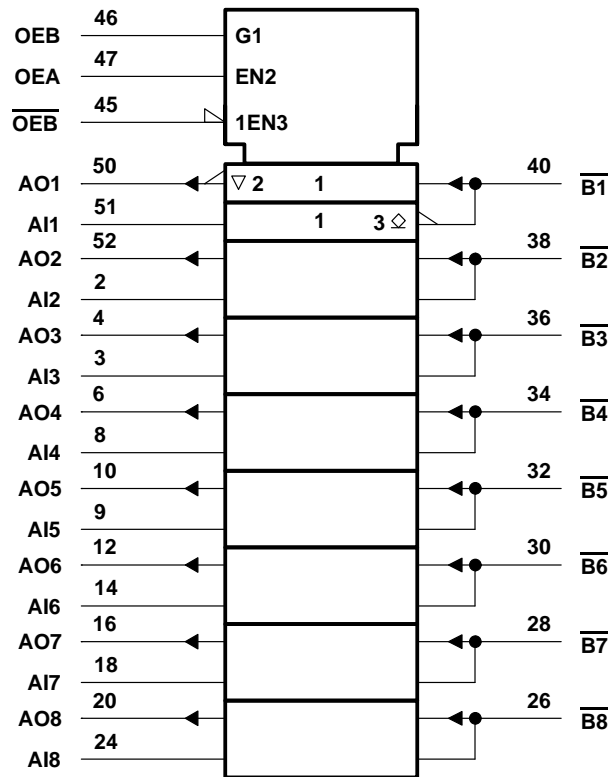
BIAS V_{CC} establishes a voltage between 1.62 V and 2.1 V on the BTL outputs when V_{CC} is not connected.

The SN54FB2040 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74FB2040 is characterized for operation from 0°C to 70°C .

FUNCTION TABLE

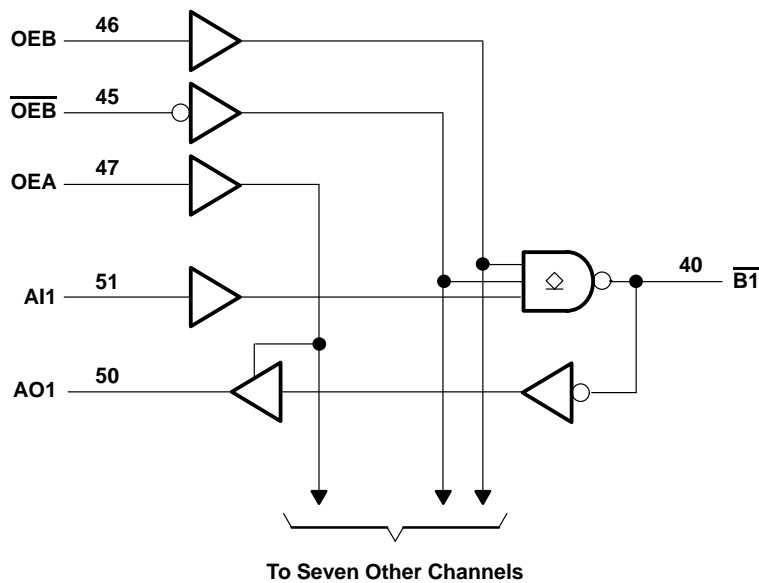
INPUTS			FUNCTION
OEB	\overline{OEB}	OEA	
L	X	L	Isolation
X	H	L	
L	X	H	\overline{B} data to AO bus
X	H	H	
H	L	L	\overline{A} data to B bus
H	L	H	\overline{A} data to B bus, \overline{B} data to AO bus

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the RC package.

functional block diagram



Pin numbers shown are for the RC package.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Voltage range applied to any \bar{B} output in the disabled or power-off state, V_O	–0.5 V to 3.5 V
Voltage range applied to any output in the high state, V_O : A port	–0.5 V to V_{CC}
Input voltage range, V_I : Except \bar{B} port	–1.2 V to 7 V
\bar{B} port	–1.2 V to 3.5 V
Input clamp current, I_{IK} : Except \bar{B} port	–40 mA
\bar{B} port	–18 mA
Current applied to any single output in the low state, I_O : A port	48 mA
\bar{B} port	200 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 1): RC package	1.4 W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 75 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 2)

		SN54FB2040			SN74FB2040			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} , BIAS V_{CC} , BG V_{CC}	Supply voltage	4.75	5	5.25	4.5	5	5.5	V
V_{IH}	High-level input voltage	\bar{B} port*		2.3	\bar{B} port*		2.3	V
		Except \bar{B} port		2	Except \bar{B} port		2	
V_{IL}	Low-level input voltage	\bar{B} port*		1.47	\bar{B} port*		1.47	V
		Except \bar{B} port		0.8	Except \bar{B} port		0.8	
I_{IK}	Input clamp current	–18			–18			mA
I_{OH}	High-level output current	AO port			AO port		–3	mA
I_{OL}	Low-level output current	AO port			AO port		24	mA
		\bar{B} port		100	\bar{B} port		100	
T_A	Operating free-air temperature	–55		125	0		70	°C

* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not tested.

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54FB2040			SN74FB2040			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{IK}	B̄ port	V _{CC} = 4.5 V	I _I = −18 mA	−1.2			−1.2			V
	Except B̄ port		I _I = −40 mA	−1.2			−0.5			
V _{OH}	AO port	V _{CC} = 4.5 V	I _{OH} = −1 mA	3.2						V
			I _{OH} = −3 mA	2.5	3.3	2.5	3.3			
V _{OL}	AO port	V _{CC} = 4.5 V	I _{OL} = 20 mA	0.09						V
			I _{OL} = 24 mA	0.35	0.5	0.35	0.5			
	B̄ port	V _{CC} = 4.5 V	I _{OL} = 80 mA	0.75	1.1	0.75	1.1			
			I _{OL} = 100 mA	1.2	1.15					
I _I	Except B̄ port	V _{CC} = 5.5 V, V _I = 5.5 V	50			50			μA	
I _{IH} ‡	Except B̄ port	V _{CC} = 5.5 V, V _I = 2.7 V	50			50			μA	
I _{IL} ‡	Except B̄ port	V _{CC} = 5.5 V	V _I = 0.5 V	−50			−50			μA
	B̄ port		V _I = 0.75 V	−100			−100			
I _{OH}	B̄ port	V _{CC} = 0 to 5.5 V, V _O = 2.1 V	100			100			μA	
I _{OZH}	AO port	V _{CC} = 5.5 V, V _O = 2.7 V	50			50			μA	
I _{OZL}	AO port	V _{CC} = 5.5 V, V _O = 0.5 V	−50			−50			μA	
I _{OZPU}	A port	V _{CC} = 0 to 2.1 V, V _O = 0.5 V to 2.7 V	50			50			μA	
I _{OZPD}	A port	V _{CC} = 2.1 V to 0, V _O = 0.5 V to 2.7 V	−50			−50			μA	
I _{OS} §	AO port	V _{CC} = 5.5 V, V _O = 0	−30	−170	−30	−180	mA			
I _{CC}	AI port to B̄ port	V _{CC} = 5.5 V, I _O = 0	25	40	40			mA		
	B̄ port to AO port		60	70	70					
C _i	AI port*	V _I = V _{CC} or GND	25	70	3.5			pF		
	Control inputs*		9.9			3				
C _O	AO port*	V _O = V _{CC} or GND		14.7			6			pF
C _{io}	B̄ port per P1194.0*	V _{CC} = 0 to 4.5 V		8#			5			pF
		V _{CC} = 4.5 V to 5.5 V		9#			5			

* On products compliant to MIL-STD-883C, Class B, this parameter is based on characterization data but is not tested.

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

Parameter does not meet P1194.0 specification.

live-insertion specifications over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		SN54FB2040		SN74FB2040		UNIT
				MIN	MAX	MIN	MAX	
I_{CC} (BIAS V_{CC})		$V_{CC} = 0\text{ to }4.5\text{ V}$	$V_B = 0\text{ to }2\text{ V}$, V_I (BIAS V_{CC}) = $4.5\text{ V to }5.5\text{ V}$		450		450	μA
		$V_{CC} = 4.5\text{ to }5.5\text{ V}$			10		10	
V_O	\overline{B} port	$V_{CC} = 0$,	V_I (BIAS V_{CC}) = 5 V	1.62	2.1	1.62	2.1	V
I_O	\overline{B} port	$V_{CC} = 0$,	$V_B = 1\text{ V}$, V_I (BIAS V_{CC}) = $4.5\text{ V to }5.5\text{ V}$	-30		-1		μA
		$V_{CC} = 0\text{ to }5.5\text{ V}$,	$OEB = 0\text{ to }0.8\text{ V}$		100		100	
		$V_{CC} = 0\text{ to }2.2\text{ V}$,	$OEB = 0\text{ to }5\text{ V}$		100		100	



SN54FB2040, SN74FB2040

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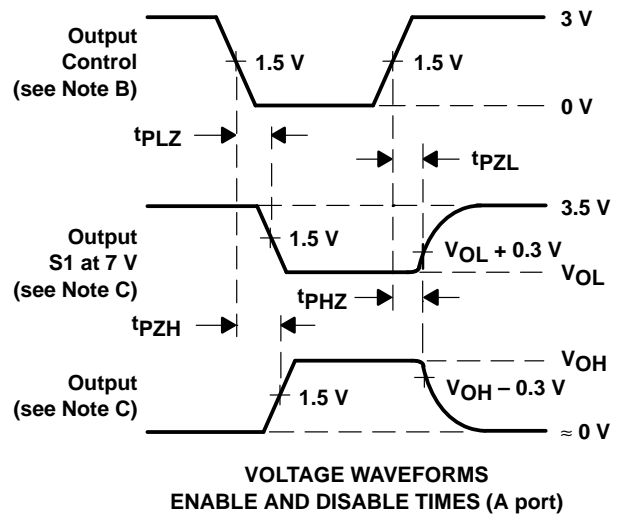
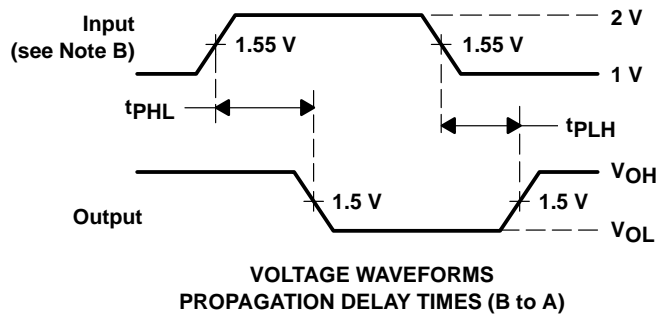
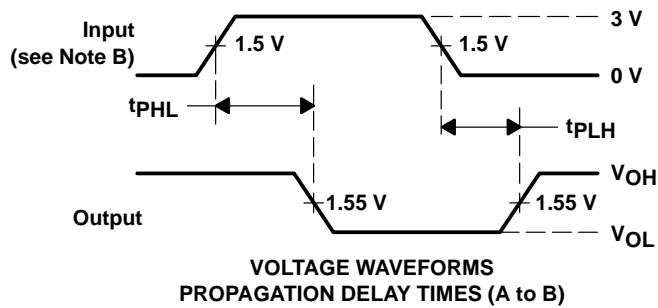
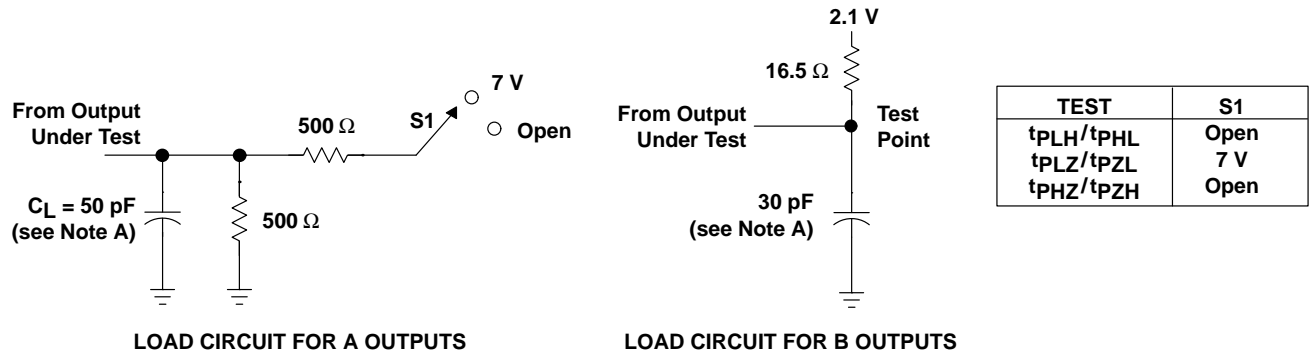
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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, T _A = 25°C			SN54FB2040		SN74FB2040		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}		AI	\overline{B}	3.2	4.5	6	0.5	8.5	2.4	6.5	ns
t _{PHL}				2.8	4.2	5.6	0.4	8.5	2.7	5.8	
t _{PLH}		\overline{B}	AO	2.3	3.8	5.7	0.4	8	1.9	6.2	ns
t _{PHL}				2.3	4.2	5.9	0.8	14.9	2	8.2	
t _{PLH}		OEB	\overline{B}	3.7	5.1	6.7	0.5	9.9	3	7	ns
t _{PHL}				3.1	4.6	5.9	0.4	9.5	3	6.1	
t _{PLH}		\overline{OEB}	\overline{B}	3.6	5.2	6.8	1.3	9.5	3.3	7	ns
t _{PHL}				2.9	4.4	5.9	0.2	9.8	2.6	6.1	
t _{PZH}		OEA	AO	2.5	4	5.5	1.2	8	2.1	5.8	ns
t _{PZL}				2.1	3.6	4.8	0.8	7.5	2	5	
t _{PHZ}		OEA	AO	2.3	4.1	5.9	1	8.2	1.9	6.5	ns
t _{PLZ}				1.6	3.1	4.5	0.4	7.2	1.4	4.7	
t _{sk(p)*}	Skew for any single channel t _{PHL} – t _{PLH} , AI to \overline{B} or \overline{B} to AO			0.5							ns
t _{sk(o)*}	Skew between drivers in the same package, AI to \overline{B} or \overline{B} to AO			0.4			2				ns
t _r	Rise time, 1.3 V to 1.8 V, \overline{B} port			2	2.8	3.8	0.2	4.5	1.7		
t _f	Fall time, 1.8 V to 1.3 V, \overline{B} port			1	1.9	3	0.9	4.0	1	4.2	
\overline{B} -port input pulse rejection									1	3.4	ns

* On products compliant to MIL-STD-883C, Class B, this parameter is based on characterization data but is not tested.

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
- B. All input pulses are supplied by generators having the following characteristics: TTL inputs: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$; BTL inputs: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

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