

SN54ABT126, SN74ABT126 QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

SCBS183A – FEBRUARY 1991 – REVISED JULY 1994

- State-of-the-Art *EPIC-II^B*™ BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce) < 1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- High-Drive Outputs (–32-mA I_{OH} , 64-mA I_{OL})
- Package Options Include Plastic Small-Outline (D) and Shrink Small-Outline (DB) Packages, Ceramic Chip Carriers (FK), and Plastic (N) and Ceramic (J) DIPs

description

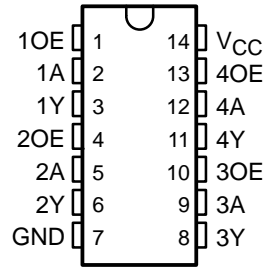
The 'ABT126 bus buffer gates feature independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable (OE) input is low.

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

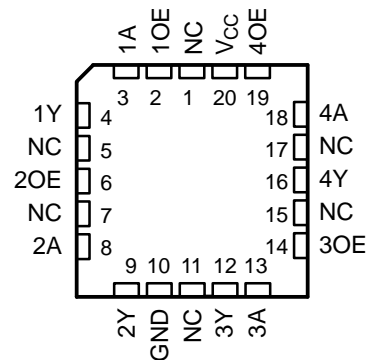
The SN74ABT126 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54ABT126 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ABT126 is characterized for operation from -40°C to 85°C .

SN54ABT126 . . . J PACKAGE
SN74ABT126 . . . D, DB, OR N PACKAGE
(TOP VIEW)



SN54ABT126 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT Y
OE	A	
H	H	H
H	L	L
L	X	Z

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UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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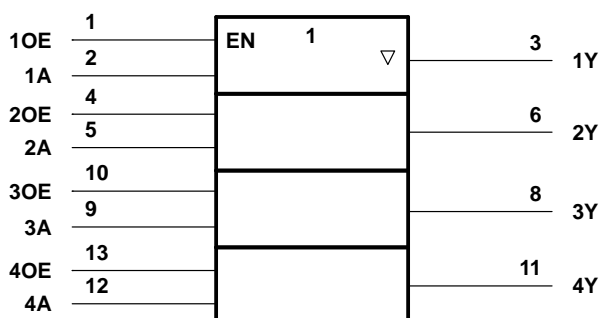
SN54ABT126, SN74ABT126

QUADRUPLE BUS BUFFER GATES

WITH 3-STATE OUTPUTS

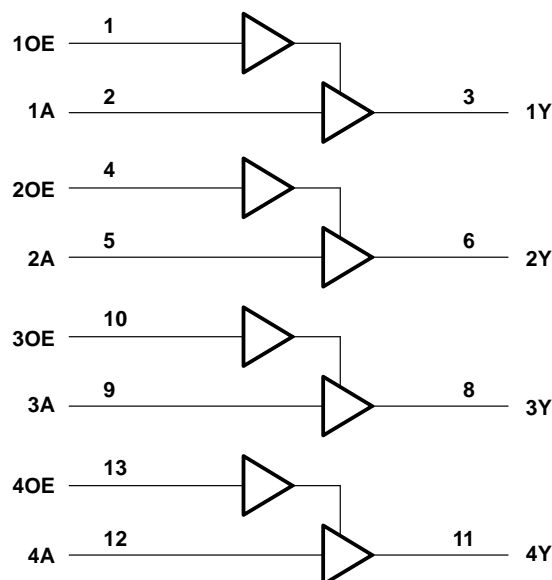
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O	–0.5 V to 5.5 V
Current into any output in the low state, I_O : SN54ABT126	96 mA
SN74ABT126	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	–18 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2): D package	1.25 W
DB package	0.5 W
N package	1.1 W
Storage temperature range	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

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recommended operating conditions (see Note 3)

		SN54ABT126		SN74ABT126		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–24		–32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		10		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		μ s/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A = 25^\circ\text{C}$			SN54ABT126		SN74ABT126		UNIT
					MIN	MAX	MIN	MAX	
V_{IK}	$V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$			–1.2		–1.2		–1.2	V
V_{OH}	$V_{CC} = 4.5\text{ V}$, $I_{OH} = -3\text{ mA}$	2.5			2.5		2.5		V
	$V_{CC} = 5\text{ V}$, $I_{OH} = -3\text{ mA}$	3			3		3		
	$V_{CC} = 4.5\text{ V}$	$I_{OH} = -24\text{ mA}$	2		2				
		$I_{OH} = -32\text{ mA}$	2*				2		
V_{OL}	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 48\text{ mA}$		0.55		0.55			V
		$I_{OL} = 64\text{ mA}$		0.55*				0.55	
I_I	$V_{CC} = 0\text{ to }5.5\text{ V}$, $V_I = V_{CC}\text{ or GND}$			± 1		± 1		± 1	μ A
I_{OZPU}	$V_{CC} = 0\text{ to }2.1\text{ V}$, $V_O = 0.5\text{ V to }2.7\text{ V}$, $OE = X$			± 50		± 50		± 50	μ A
I_{OZPD}	$V_{CC} = 2.1\text{ V to }0$, $V_O = 0.5\text{ V to }2.7\text{ V}$, $OE = X$			± 50		± 50		± 50	μ A
I_{OZH}	$V_{CC} = 2.1\text{ V to }5.5\text{ V}$, $V_O = 2.7\text{ V}$, $OE \leq 0.8\text{ V}^\ddagger$			10		10		10	μ A
I_{OZL}	$V_{CC} = 2.1\text{ V to }5.5\text{ V}$, $V_O = 0.5\text{ V}$, $OE \leq 0.8\text{ V}^\ddagger$			–10		–10		–10	μ A
I_{off}	$V_{CC} = 0$, $V_I\text{ or }V_O \leq 4.5\text{ V}$			± 100				± 100	μ A
I_{CEX}	$V_{CC} = 5.5\text{ V}$, $V_O = 5.5\text{ V}$		Outputs high	50		50		50	μ A
I_O^\S	$V_{CC} = 5.5\text{ V}$, $V_O = 2.5\text{ V}$	–50	–100	–200	–50	–200	–50	–200	mA
I_{CC}	$V_{CC} = 5.5\text{ V}$, $V_I = V_{CC}\text{ or GND}$ $I_O = 0$	Outputs high		1	250		250		μ A
		Outputs low		24	30		30		mA
		Outputs disabled		0.5	250		250		μ A
ΔI_{CC}^\P	$V_{CC} = 5.5\text{ V}$, One input at 3.4 V, Other inputs at $V_{CC}\text{ or GND}$	Outputs enabled			1.5		1.5		mA
		Outputs disabled			50		50		μ A
C_i	$V_I = 2.5\text{ V or }0.5\text{ V}$			3					pF
C_o	$V_O = 2.5\text{ V or }0.5\text{ V}$			7					pF

* On products compliant to MIL-STD-883, Class B, this parameter does not apply.

† All typical values are at $V_{CC} = 5\text{ V}$.

‡ For V_{CC} between 2.1 V and 4 V, OE should be less than or equal to 0.5 V to ensure a low state.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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QUADRUPLE BUS BUFFER GATES

WITH 3-STATE OUTPUTS

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$			SN54ABT126		SN74ABT126		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}^\dagger	A	Y	1	2.9	4.9	1	7.3	1	6.3	ns
t_{PHL}^\dagger			1	2.5	5.1	1	5.9	1	5.7	
t_{PZH}^\dagger	OE	Y	1	4.4	5.8	1	5.3	1	6.5	ns
t_{PZL}^\dagger			1	4.4	5.9	1	6.4	1	6.5	
t_{PHZ}^\dagger	OE	Y	1	3	5.7	1	6.9	1	6.8	ns
t_{PLZ}^\dagger			1	3	5.8	1	7.2	1	6.7	

[†] This data sheet limit may vary among suppliers.

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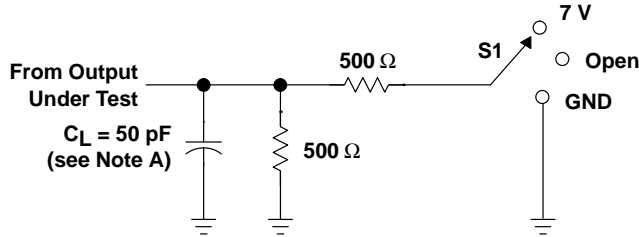


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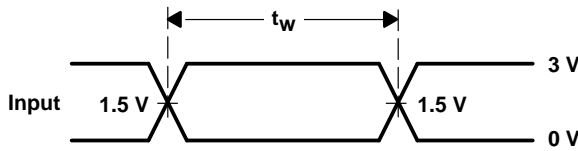
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PARAMETER MEASUREMENT INFORMATION

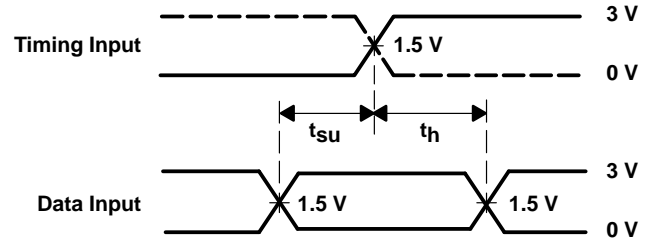


LOAD CIRCUIT FOR OUTPUTS

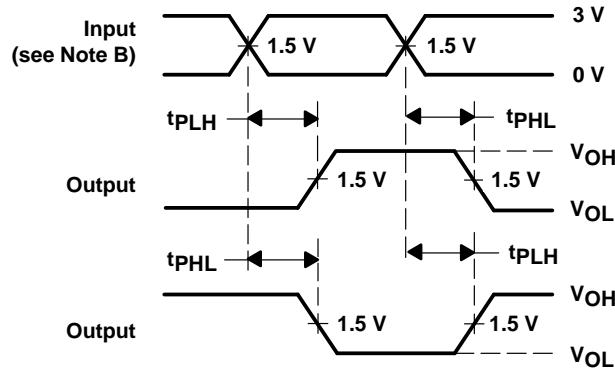
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



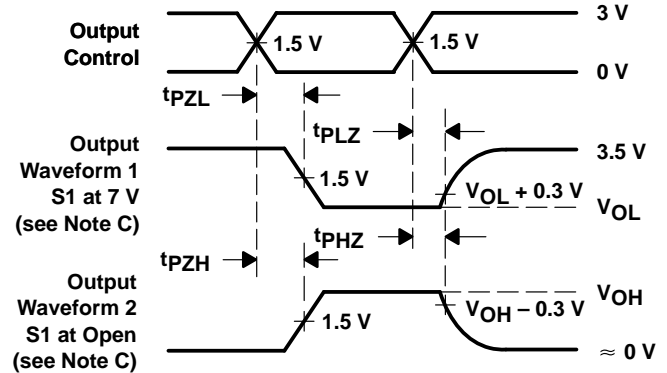
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- C_L includes probe and jig capacitance.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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