

SN54ABT843, SN74ABT843 9-BIT BUS-INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCBS197B – FEBRUARY 1991 – REVISED JULY 1994

- State-of-the-Art *EPIC-II B*™ BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce) < 1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- High-Drive Outputs ($-32\text{-mA } I_{OH}$, $64\text{-mA } I_{OL}$)
- Package Options Include Plastic Small-Outline (DW) and Shrink Small-Outline (DB) Packages, Ceramic Chip Carriers (FK), and Plastic (NT) and Ceramic (JT) DIPs

description

The 'ABT843 9-bit latches are designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The nine latches are transparent D-type latches. The device has noninverting data (D) inputs and provides true data at its outputs.

A buffered output-enable (\overline{OE}) input can be used to place the nine outputs in either a normal logic state (high or low levels) or a high-impedance state. The outputs are also in the high-impedance state during power-up and power-down conditions. The outputs remain in the high-impedance state while the device is powered-down. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

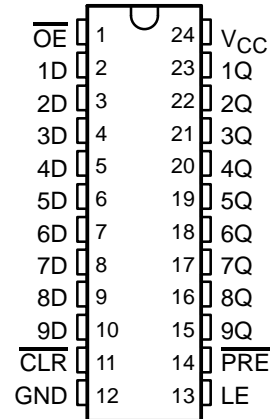
\overline{OE} does not affect the internal operations of the latch. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

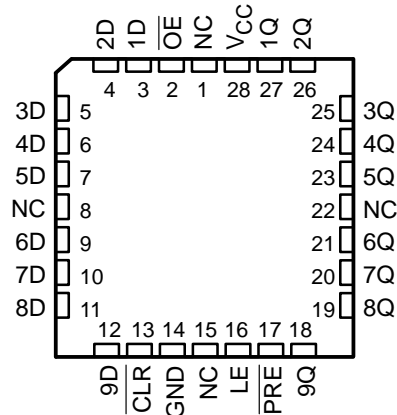
The SN74ABT843 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54ABT843 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ABT843 is characterized for operation from -40°C to 85°C .

SN54ABT843 . . . JT PACKAGE
SN74ABT843 . . . DB, DW, OR NT PACKAGE
(TOP VIEW)



SN54ABT843 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

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**TEXAS
INSTRUMENTS**

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SN54ABT843, SN74ABT843

9-BIT BUS-INTERFACE D-TYPE LATCHES

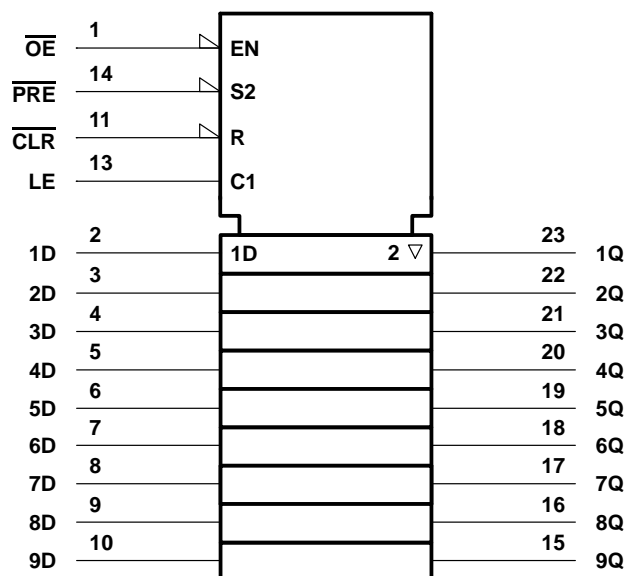
WITH 3-STATE OUTPUTS

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FUNCTION TABLE

INPUTS					OUTPUT Q
PRE	CLR	OE	LE	D	
L	X	L	X	X	H
H	L	L	X	X	L
H	H	L	H	L	L
H	H	L	H	H	H
H	H	L	L	X	Q ₀
X	X	H	X	X	Z

logic symbol†

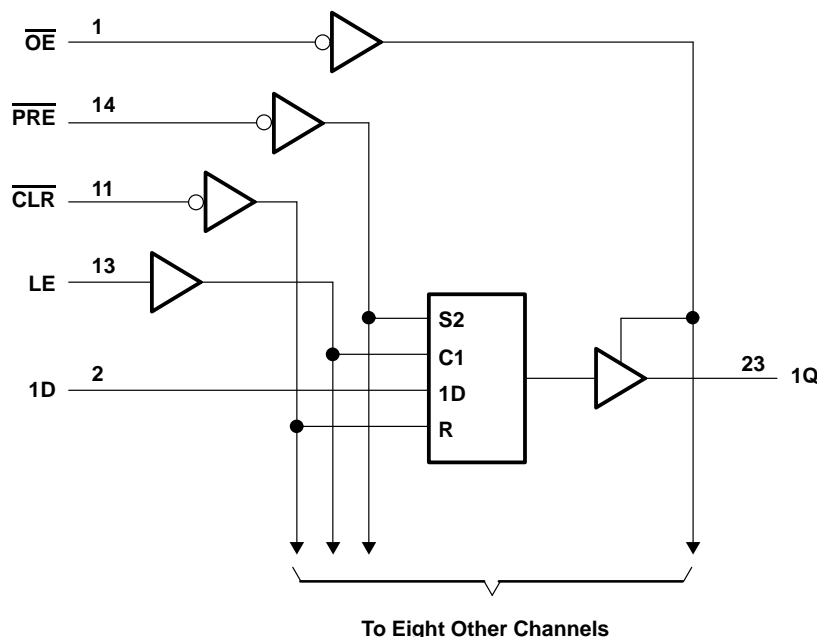


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DB, DW, JT, and NT packages.

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logic diagram (positive logic)



Pin numbers shown are for the DB, DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O	–0.5 V to 5.5 V
Current into any output in the low state, I_O : SN54ABT843	96 mA
SN74ABT843	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	–18 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2): DB package	0.65 W
DW package	1.7 W
NT package	1.3 W
Storage temperature range	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the “recommended operating conditions” section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the NT package, which has a trace length of zero. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

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recommended operating conditions (see Note 3)

		SN54ABT843		SN74ABT843		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–24		–32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		5		5	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A = 25^\circ\text{C}$			SN54ABT843		SN74ABT843		UNIT
		MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	$V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$			–1.2		–1.2		–1.2	V
V_{OH}	$V_{CC} = 4.5\text{ V}$, $I_{OH} = -3\text{ mA}$	2.5			2.5		2.5		V
	$V_{CC} = 5\text{ V}$, $I_{OH} = -3\text{ mA}$	3			3		3		
	$V_{CC} = 4.5\text{ V}$				2				
							2		
V_{OL}	$V_{CC} = 4.5\text{ V}$				0.55				V
				0.55*			0.55		
I_I	$V_{CC} = 5.5\text{ V}$, $V_I = V_{CC}$ or GND			± 1		± 1		± 1	μA
I_{OZH}^\ddagger	$V_{CC} = 5.5\text{ V}$, $V_O = 2.7\text{ V}$			10		10		10	μA
I_{OZL}^\ddagger	$V_{CC} = 5.5\text{ V}$, $V_O = 0.5\text{ V}$			–10		–10		–10	μA
I_{off}	$V_{CC} = 0$, V_I or $V_O \leq 4.5\text{ V}$			± 100				± 100	μA
I_{CEX}	$V_{CC} = 5.5\text{ V}$, $V_O = 5.5\text{ V}$			50		50		50	μA
I_O^\S	$V_{CC} = 5.5\text{ V}$, $V_O = 2.5\text{ V}$	–50	–140	–180	–50	–180	–50	–180	mA
I_{CC}	$V_{CC} = 5.5\text{ V}$, $I_O = \text{Open}$, $V_I = V_{CC}$ or GND			1	250		250		μA
				24	34		34		mA
				0.5	250		250		μA
ΔI_{CC}^\P	$V_{CC} = 5.5\text{ V}$, One input at 3.4 V, Other inputs at V_{CC} or GND			1.5		1.5		1.5	mA
C_i	$V_I = 2.5\text{ V}$ or 0.5 V			4					pF
C_o	$V_O = 2.5\text{ V}$ or 0.5 V			7					pF

* On products compliant to MIL-STD-883, Class B, this parameter does not apply.

† All typical values are at $V_{CC} = 5\text{ V}$.

‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figures 1 and 2)

			V _{CC} = 5 V, T _A = 25°C		SN54ABT843		SN74ABT843		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration	CLR low	5.5		5.5		5.5		ns
		PRE high	4.5		4.5		4.5		
		LE low	3.3		3.3		3.4		
t _{su}	Setup time	Data before LE↓	Low	2.5	2.5		2.5		ns
			High	3	3		3		
		PRE inactive	1.6		1.6		1.6		
		CLR inactive	2		2		2		
t _h	Hold time, data after LE↓	High	1		1		1		ns
		Low	1.5†		1.5†		1.5†		

† This data sheet limit may vary among suppliers.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, T _A = 25°C			SN54ABT843		SN74ABT843		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	D	Q	1.2†	3.8	5.2	1.2†	7.8	1.2†	6.7†	ns
t _{PHL}			1.5†	3.4	6.3	1.5†	7.3	1.5†	7.2	
t _{PLH}	LE	Q	1.7†	4.4	5.6	1.7†	8.3	1.7†	7.2†	ns
t _{PHL}			1.9†	4.1	6.3	1.9†	7.2	1.9†	6.9	
t _{PLH}	PRE	Q	2.2	5	6.2	2.2	8	2.2	7.4	ns
t _{PHL}			2.1†	4.1	6.5	2.1†	7.5	2.1†	7.2	
t _{PLH}	CLR	Q	2†	4.4	6.3	2†	7.6	2†	7.1	ns
t _{PHL}			1.9†	4.5	6.8	1.9†	8.1	1.9†	8	
t _{PZH}	OE	Q	1	3.4	4.5†	1	5.9	1	5.7†	ns
t _{PZL}			2	4.3	5.7†	2	6.6	2	6.5	
t _{PHZ}	OE	Q	2.4†	4.9	6.2	2.4†	7	2.4†	6.8	ns
t _{PLZ}			1.5†	4.2	6.3	1.5†	6.4	1.5†	5.9†	

† This data sheet limit may vary among suppliers.

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recovery-time waveform

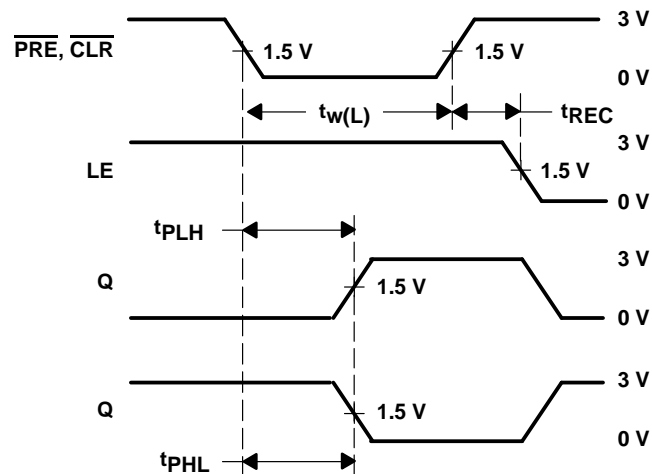
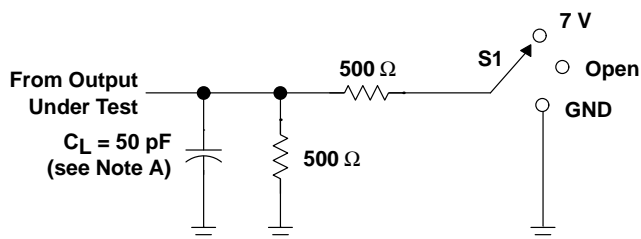


Figure 1. \overline{CLR} and \overline{PRE} Pulse Duration, \overline{CLR} and \overline{PRE} to Output Delay, and \overline{CLR} and \overline{PRE} to Latch-Enable Recovery Time

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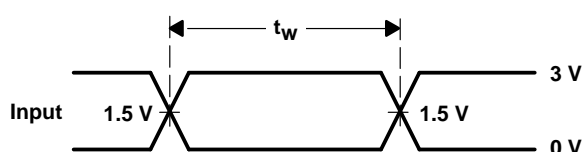
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PARAMETER MEASUREMENT INFORMATION

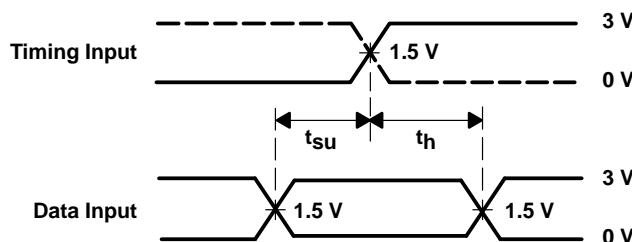


LOAD CIRCUIT FOR OUTPUTS

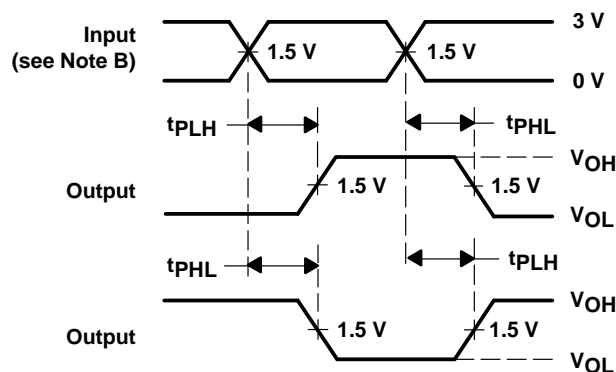
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



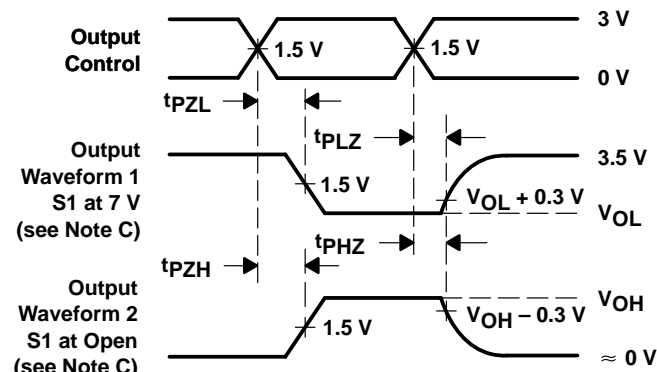
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

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