

SN54ABT853, SN74ABT853 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS

SCBS198C – FEBRUARY 1991 – REVISED JANUARY 1996

- State-of-the-Art **EPIC-IITM** BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce) < 1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- High-Drive Outputs (–32-mA I_{OH} , 64-mA I_{OL})
- Parity Error Flag With Parity Generator/Checker
- Latch for Storage of the Parity Error Flag
- Package Options Include Plastic Small-Outline (DW) and Shrink Small-Outline (DB) Packages, Ceramic Chip Carriers (FK), and Plastic (NT) and Ceramic (JT) DIPs

description

The 'ABT853 8-bit to 9-bit parity transceivers are designed for communication between data buses. When data is transmitted from the A bus to the B bus, a parity bit is generated. When data is transmitted from the B bus to the A bus with its corresponding parity bit, the open-collector parity-error (\overline{ERR}) output indicates whether or not an error in the B data has occurred. The output-enable ($\overline{OE_A}$ and $\overline{OE_B}$) inputs can be used to disable the device so that the buses are effectively isolated. The 'ABT853 transceivers provide true data at their outputs.

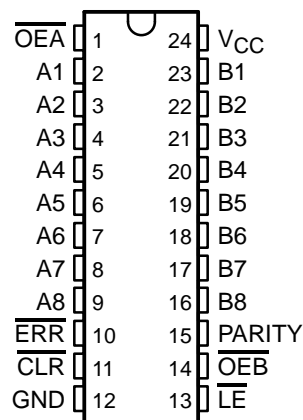
A 9-bit parity generator/checker generates a parity-odd (PARITY) output and monitors the parity of the I/O ports with the \overline{ERR} flag. The parity-error output can be passed, sampled, stored, or cleared from the latch using the latch-enable (\overline{LE}) and clear (\overline{CLR}) control inputs. When both $\overline{OE_A}$ and $\overline{OE_B}$ are low, data is transferred from the A bus to the B bus and inverted parity is generated. Inverted parity is a forced error condition that gives the designer more system diagnostic capability.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

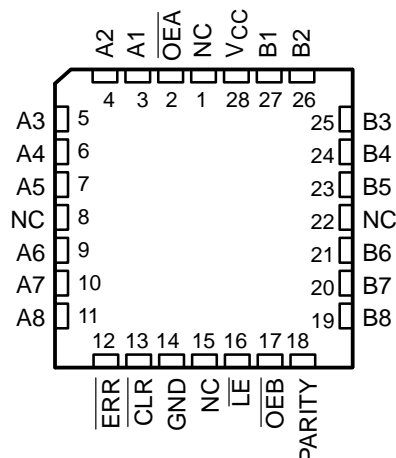
The SN74ABT853 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54ABT853 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ABT853 is characterized for operation from -40°C to 85°C .

SN54ABT853 . . . JT PACKAGE
SN74ABT853 . . . DB, DW, OR NT PACKAGE
(TOP VIEW)



SN54ABT853 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection



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**TEXAS
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FUNCTION TABLE

INPUTS						OUTPUTS AND I/OS				FUNCTION
$\overline{\text{OEB}}$	$\overline{\text{OEA}}$	$\overline{\text{CLR}}$	LE	Ai Σ OF H	Bi† Σ OF H	A	B	PARITY	$\overline{\text{ERR}}‡$	
L	H	X	X	Odd Even	NA	NA	A	L H	NA	A data to B bus and generate parity
H	L	X	L	NA	Odd Even	B	NA	NA	H L	B data to A bus and check parity
H	L	H	H	NA	X	X	NA	NA	NC	Store error flag
X	X	L	H	X	X	X	NA	NA	H	Clear error flag register
H	H	H	H	X	X	Z	Z	Z	NC	Isolation§ (parity check)
		L	H	X					H	
		X	L	L Odd					H	
		X	L	H Even					L	
L	L	X	X	Odd Even	NA	NA	A	H L	NA	A data to B bus and generate inverted parity

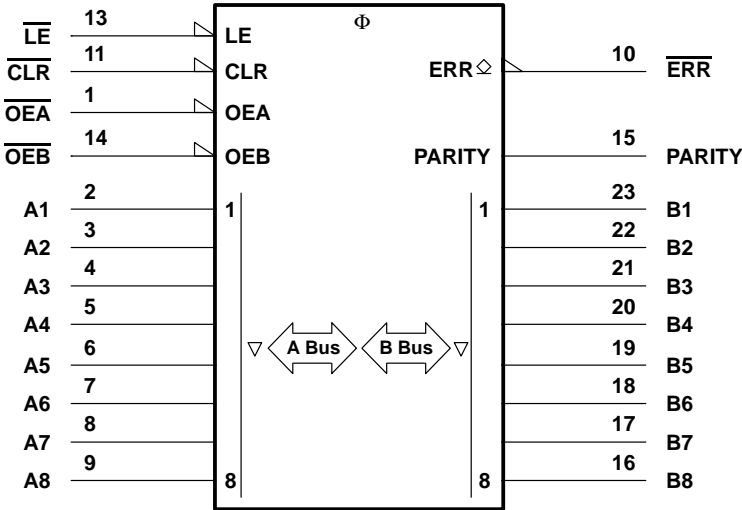
NA = not applicable, NC = no change, X = don't care

† Summation of high-level inputs includes PARITY along with Bi inputs.

‡ Output states shown assume the ERR output was previously high.

§ In this mode, the ERR output (when clocked) shows inverted parity of the A bus.

logic symbol¶

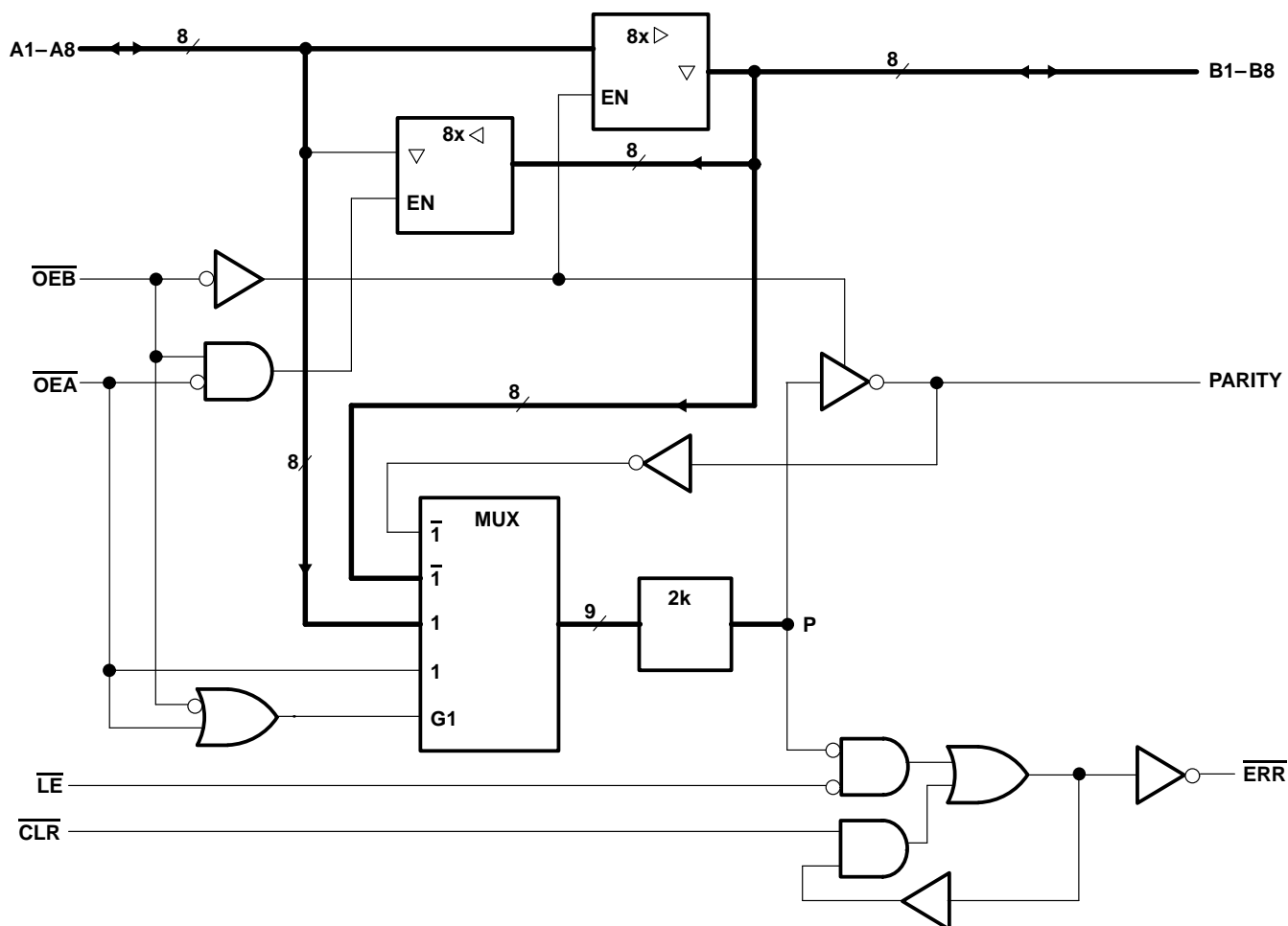


¶ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the DB, DW, JT, and NT packages.

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logic diagram (positive logic)



ERROR-FLAG FUNCTION TABLE

INPUTS		INTERNAL TO DEVICE	OUTPUT PRESTATE	OUTPUT ERR	FUNCTION
CLR	LE	POINT P	$\overline{\text{ERR}}_{N-1}^{\dagger}$		
L	L	L	X	L	Pass
		H	X	H	
H	L	L	X	L	Sample
		H	H	H	
L	H	X	X	H	Clear
H	H	X	L	L	Store
			H	H	

[†] The state of the ERR output before any changes at CLR, LE, or point P

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Timing diagram for the 74VHC163 4-bit counter. The diagram shows the waveforms for OEB, OEA, Bi + PARITY, LE, CLR, and ERR signals over time. The OEB and OEA signals are active-low and remain high. The Bi + PARITY signal is a periodic square wave. The LE signal is active-low and pulses high during the 'Store' phase. The CLR signal is active-low and pulses high during the 'Clear' phase. The ERR signal is active-low and pulses high during the 'Pass' and 'Clear' phases. The diagram is divided into three phases: Pass, Store, and Clear. The 'Pass' phase is marked by a double-headed arrow. The 'Store' phase is marked by a double-headed arrow. The 'Clear' phase is marked by a double-headed arrow. The 'Sample' phase is marked by a single-headed arrow.

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1)	−0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O	−0.5 V to 5.5 V
Current into any output in the low state, I_O : SN54ABT853	96 mA
SN74ABT853	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	−18 mA
Output clamp current, I_{OK} ($V_O < 0$)	−50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2): DB package	0.65 W
DW package	1.7 W
NT package	1.3 W
Storage temperature range, T_{stg}	−65°C to 150°C

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the NT package, which has a trace length of zero. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

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recommended operating conditions (see Note 3)

		SN54ABT853		SN74ABT853		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_{OH}	High-level output voltage	\overline{ERR}		5.5		V
I_{OH}	High-level output current	Except \overline{ERR}		–32		mA
I_{OL}	Low-level output current			64		mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		$\mu s/V$
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused or floating pins (input or I/O) must be held high or low.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T _A = 25°C			SN54ABT853		SN74ABT853		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V _{IK}		V _{CC} = 4.5 V, I _I = -18 mA				-1.2		-1.2		-1.2	V
V _{OH}	All outputs except $\overline{\text{ERR}}$	V _{CC} = 4.5 V, I _{OH} = -3 mA		2.5			2.5		2.5		V
		V _{CC} = 5 V, I _{OH} = -3 mA		3			3		3		
		V _{CC} = 4.5 V	I _{OH} = -24 mA	2			2				
			I _{OH} = -32 mA	2*					2		
V _{OL}		V _{CC} = 4.5 V	I _{OL} = 24 mA			0.55		0.55			V
			I _{OL} = 64 mA			0.55*				0.55	
I _{OH}	$\overline{\text{ERR}}$	V _{CC} = 4.5 V, V _{OH} = 5.5 V				50		50		50	μA
I _I	Control inputs	V _{CC} = 5.5 V, V _I = V _{CC} or GND				±1		±1		±1	μA
	A or B ports					±100		±100		±100	
I _{OZ}	Power up	V _{CC} = 0 to 2.1 V	V _O = 0.5 V to 2.7 V, OE = X			±50		±50		±50	μA
I _{OZ}	Power down	V _{CC} = 2.1 V to 0				±50		±50		±50	μA
I _{OZH} ‡		V _{CC} = 5.5 V, V _O = 2.7 V				10		10		10	μA
I _{OZL} ‡		V _{CC} = 5.5 V, V _O = 0.5 V				-10		-10		-10	μA
I _{off}		V _{CC} = 0, V _I or V _O ≤ 4.5 V				±100				±100	μA
I _{CEX}		V _{CC} = 5.5 V, V _O = 5.5 V	Outputs high			50		50		50	μA
I _O §		V _{CC} = 5.5 V, V _O = 2.5 V		-50	-100	-200#	-50	-200#	-50	-200#	mA
I _{CC}	A or B ports	V _{CC} = 5.5 V, V _I = V _{CC} or GND	Outputs high		1	250		250		250	μA
			Outputs low		24	38		38		38	mA
			Outputs disabled		0.5	250		250		250	μA
ΔI _{CC} ¶		V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND	Data inputs			1.5		1.5		1.5	mA
			Outputs disabled			50		50		50	μA
			Control inputs			1.5		1.5		1.5	mA
C _i	Control inputs	V _I = 2.5 V or 0.5 V				4.5					pF
C _{io}	A or B ports	V _O = 2.5 V or 0.5 V				10.5					pF

* On products compliant to MIL-STD-883, Class B, this parameter does not apply.

† All typical values are at V_{CC} = 5 V.

‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			$V_{CC} = 3.3 \text{ V}, \pm 0.3 \text{ V}$		SN54ABT853		SN74ABT853		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	\overline{LE} high or low	3.5		8.5		8.5		ns
		\overline{CLR} low	4		4		4		
t_{su}	Setup time	B or PARITY before $\overline{LE}\downarrow$	9.4†		9.4†		9.4†		ns
		\overline{CLR} before $\overline{LE}\downarrow$	2		2		2		
t_h	Hold time	B or PARITY after $\overline{LE}\downarrow$	0		0		0		ns
		\overline{CLR} after $\overline{LE}\downarrow$	3		3		3		

† This data sheet limit can vary among suppliers.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$			SN54ABT853		SN74ABT853		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1.2		4.8	1.2	5.4	1.2	5.3	ns
t_{PHL}			1		4.8†	1	5.4	1	5.3†	
t_{PLH}	A	PARITY	2.1		9.5	2.1	11.3	2.1	11.2	ns
t_{PHL}			2.5		9.7	2.5	11.1	2.5	11	
t_{PLH}	\overline{OE}	PARITY	1.8		8.5	1.8	10.6	1.8	10.5	ns
t_{PHL}			2.3		8.6	2.3	10.1	2.3	10	
t_{PLH}	\overline{CLR}	\overline{ERR}	1		5.5	1	6.3	1	6.2	ns
t_{PLH}	\overline{LE}	ERR	1.8		5.1	1.8	6.1	1.8	6	ns
t_{PHL}			1†		5.8	1†	6.7	1	6.6	
t_{PLH}	B or PARITY	ERR	2		10.1	2	11.8	2	11.7	ns
t_{PHL}			2.2†		11.5	2.2†	12.9	2.2†	12.8	
t_{PZH}	\overline{OE}	A or B or PARITY	1		5.8†	1	6.8	1	6.7†	ns
t_{PZL}			1.5†		5.8	1.5†	6.8	1.5†	6.7	
t_{PHZ}	\overline{OE}	A or B or PARITY	1.8†		7.3	1.8†	8	1.8†	7.9	ns
t_{PLZ}			2.1†		7.2	2.1†	8.2	2.1†	8.1	

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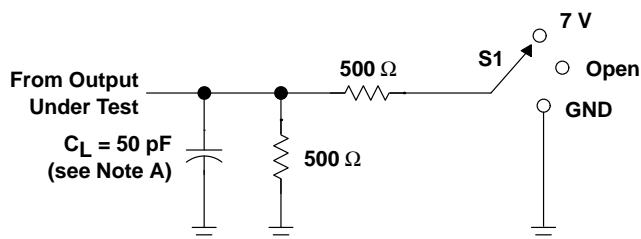


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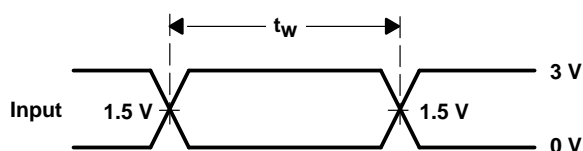
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PARAMETER MEASUREMENT INFORMATION

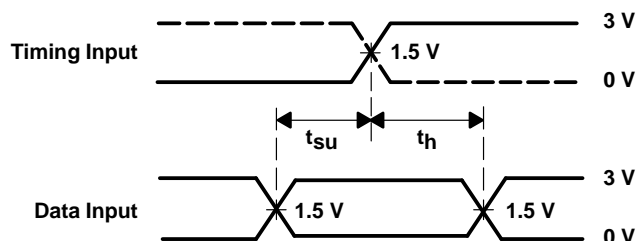


LOAD CIRCUIT FOR OUTPUTS

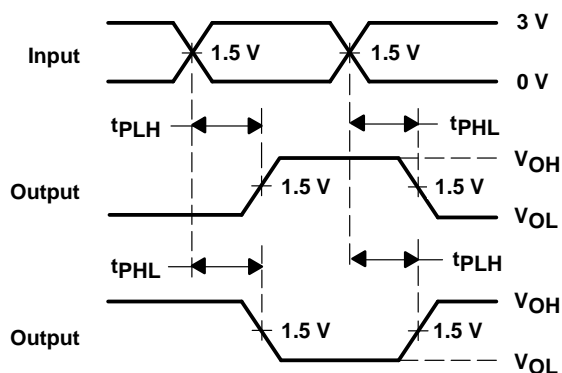
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



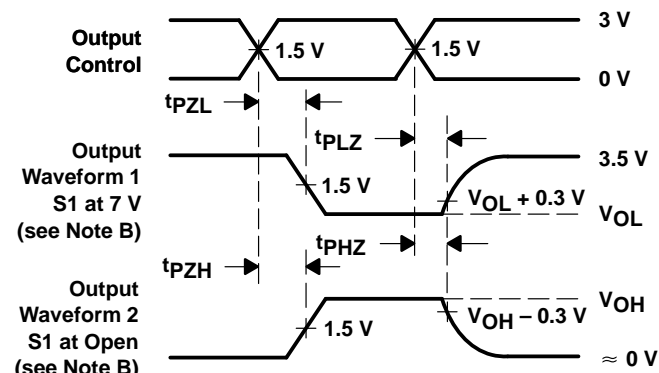
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.

D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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