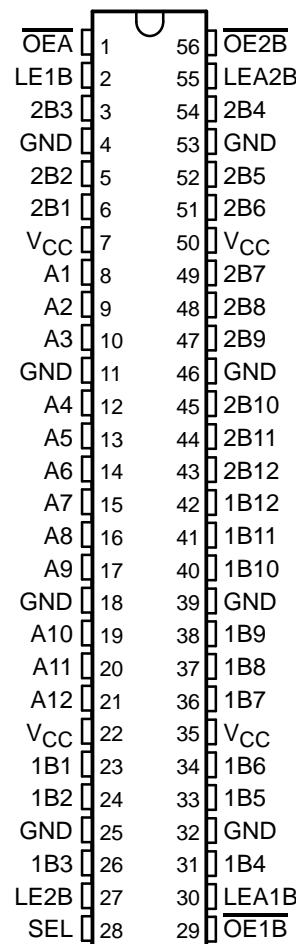


SN54ABT16260, SN74ABT16260 12-BIT TO 24-BIT MULTIPLEXED D-TYPE LATCHES WITH 3-STATE OUTPUTS

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- Members of the Texas Instruments *Widebus™* Family
- State-of-the-Art *EPIC-II B™* BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce) < 1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- High-Drive Outputs (–32-mA I_{OH} , 64-mA I_{OL})
- Bus-Hold Inputs Eliminate the Need for External Pullup Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) Package and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

SN54ABT16260 . . . WD PACKAGE
SN74ABT16260 . . . DL PACKAGE
(TOP VIEW)



description

The 'ABT16260 is a 12-bit to 24-bit multiplexed D-type latch used in applications where two separate data paths must be multiplexed onto, or demultiplexed from, a single data path. Typical applications include multiplexing and/or demultiplexing of address and data information in microprocessor- or bus-interface applications. This device is also useful in memory-interleaving applications.

Three 12-bit I/O ports (A1–A12, 1B1–1B12, and 2B1–2B12) are available for address and/or data transfer. The output-enable ($\overline{OE}1B$, $\overline{OE}2B$, and $\overline{OE}A$) inputs control the bus transceiver functions. The $\overline{OE}1B$ and $\overline{OE}2B$ control signals also allow bank control in the A to B direction.

Address and/or data information can be stored using the internal storage latches. The latch-enable (LE1B, LE2B, LEA1B, and LEA2B) inputs are used to control data storage. When the latch-enable input is high, the latch is transparent. When the latch-enable input goes low, the data present at the inputs is latched and remains latched until the latch-enable input is returned high.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT16260 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

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description (continued)

The SN54ABT16260 is characterized for operation over the full military temperature range of -55°C to 125°C .
The SN74ABT16260 is characterized for operation from -40°C to 85°C .

Function Tables

B TO A ($\overline{\text{OEB}} = \text{H}$)

INPUTS						OUTPUT A
1B	2B	SEL	LE1B	LE2B	$\overline{\text{OEA}}$	
H	X	H	H	X	L	H
L	X	H	H	X	L	L
X	X	H	L	X	L	A ₀
X	H	L	X	H	L	H
X	L	L	X	H	L	L
X	X	L	X	L	L	A ₀
X	X	X	X	X	H	Z

A TO B ($\overline{\text{OEA}} = \text{H}$)

INPUTS					OUTPUTS	
A	LEA1B	LEA2B	$\overline{\text{OE1B}}$	$\overline{\text{OE2B}}$	1B	2B
H	H	H	L	L	H	H
L	H	H	L	L	L	L
H	H	L	L	L	H	2B ₀
L	H	L	L	L	L	2B ₀
H	L	H	L	L	1B ₀	H
L	L	H	L	L	1B ₀	L
X	L	L	L	L	1B ₀	2B ₀
X	X	X	H	H	Z	Z
X	X	X	L	H	Active	Z
X	X	X	H	L	Z	Active
X	X	X	L	L	Active	Active

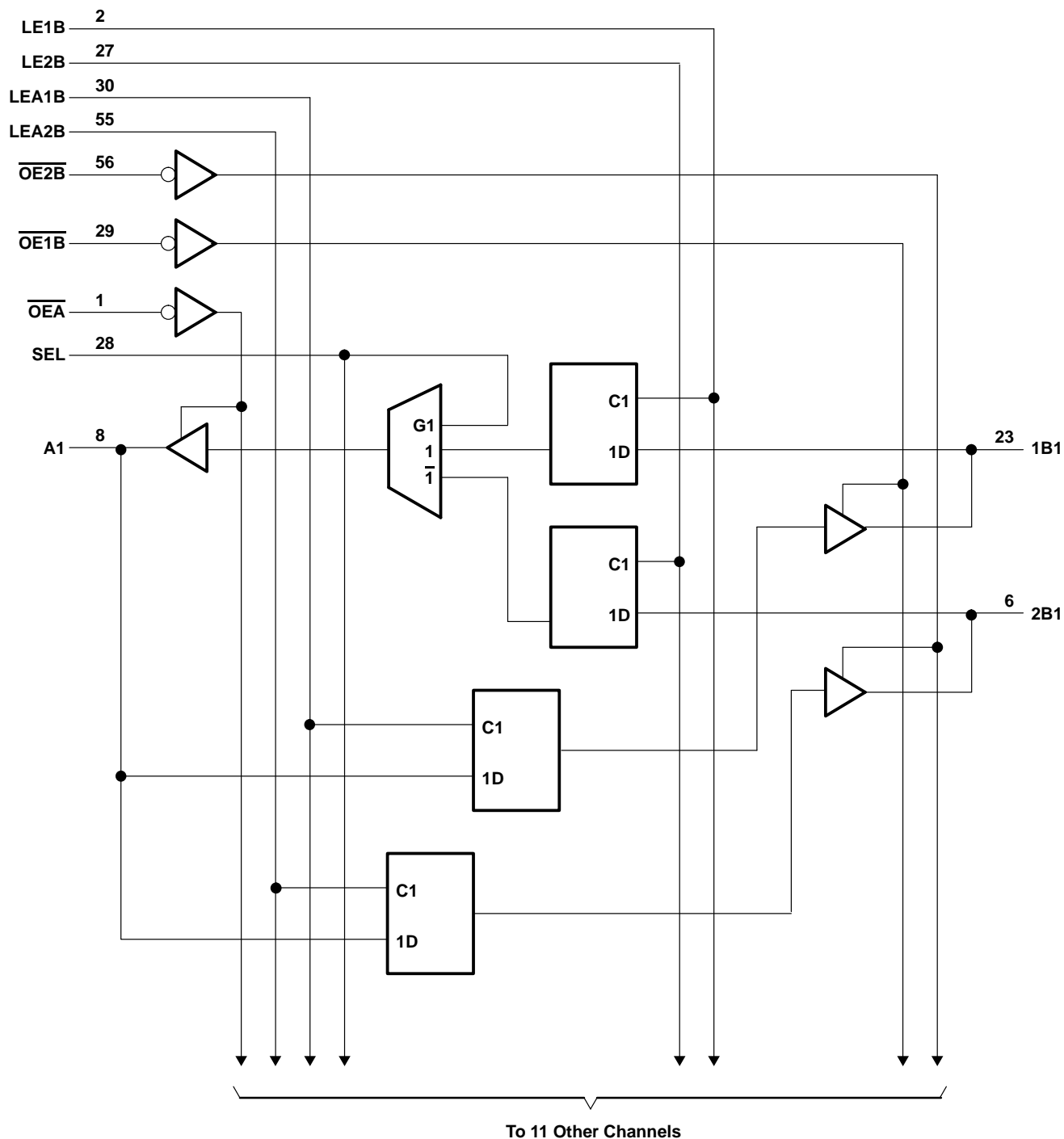
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logic diagram (positive logic)



To 11 Other Channels



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O	–0.5 V to 5.5 V
Current into any output in the low state, I_O : SN54ABT16260	96 mA
SN74ABT16260	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	–18 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2): DL package	1.4 W
Storage temperature range	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 3)

		SN54ABT16260		SN74ABT16260		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–24		–32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		μs/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused or floating inputs must be held high or low.



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12-BIT TO 24-BIT MULTIPLEXED D-TYPE LATCHES

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T _A = 25°C			SN54ABT16260		SN74ABT16260		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V _{IK}		V _{CC} = 4.5 V, I _I = –18 mA			–1.2		–1.2		–1.2	V
V _{OH}		V _{CC} = 4.5 V, I _{OH} = –3 mA	2.5			2.5		2.5		V
		V _{CC} = 5 V, I _{OH} = –3 mA	3			3		3		
		V _{CC} = 4.5 V	2			2				
			2*					2		
V _{OL}		V _{CC} = 4.5 V			0.55		0.55			V
					0.55*				0.55	
I _I	Control inputs	V _{CC} = 0 to 5.5 V, V _I = V _{CC} or GND			±1		±1		±1	μA
	A or B ports	V _{CC} = 2.1 V to 5.5 V, V _I = V _{CC} or GND			±20		±100		±20	
I _{I(hold)}	A or B ports	V _{CC} = 4.5 V, V _I = 0.8 V						100		μA
		V _{CC} = 4.5 V, V _I = 2 V						–100		
I _{OZPU}		V _{CC} = 0 to 2.1 V, V _O = 0.5 to 2.7 V, \overline{OE} = X			±50				±50	μA
I _{OZPD}		V _{CC} = 2.1 V to 0, V _O = 0.5 to 2.7 V, \overline{OE} = X			±50				±50	μA
I _{OZH} ‡		V _{CC} = 2.1 V to 5.5 V, V _O = 2.7 V, \overline{OE} ≥ 2 V			10		10		10	μA
I _{OZL} ‡		V _{CC} = 2.1 V to 5.5 V, V _O = 0.5 V, \overline{OE} ≥ 2 V			–10		–10		–10	μA
I _{off}		V _{CC} = 0, V _I or V _O ≤ 4.5 V			±100				±100	μA
I _{CEX}	Outputs high	V _{CC} = 5.5 V, V _O = 5.5 V			50		50		50	μA
I _O §		V _{CC} = 5.5 V, V _O = 2.5 V	–50	–100	–225	–50	–225	–50	–225	mA
I _{CC}	Outputs high	V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND			1.5		1.5		1.5	mA
	Outputs low				63		63		63	
	Outputs disabled				1		1		1	
ΔI _{CC} ¶		V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND			1.5		1.5		1.5	mA
C _i		V _I = 2.5 V or 0.5 V			3					pF
C _{io}		V _O = 2.5 V or 0.5 V			11.5					pF

* On products compliant to MIL-STD-883, Class B, this parameter does not apply.

† All typical values are at V_{CC} = 5 V.

‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$		SN54ABT16260		SN74ABT16260		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE1B, LE2B, LEA1B, or LEA2B high	3.3		3.3		3.3		ns
t_{su}	Setup time, data before LE1B, LE2B, LEA1B, or LEA2B↓	1.5		2		1.5		ns
t_h	Hold time, data after LE1B, LE2B, LEA1B, or LEA2B↓	1		2		1		ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$			SN54ABT16260		SN74ABT16260		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1	3.1	4.8	1	5.9	1	5.6	ns
t_{PHL}			1	3.4	5	1	6.3	1	5.9	
t_{PLH}	\overline{LE}	A or B	1.1	3.2	4.9	1.1	6.6	1.1	5.8	ns
t_{PHL}			1.1	3.3	4.9	1.1	5.9	1.1	5.3	
t_{PLH}	SEL (B1)	A	1.3	3.2	4.6	1.3	5.4	1.3	5.3	ns
	SEL (B2)		1.1	3.4	4.9	1.1	6.3	1.1	6	
t_{PHL}	SEL (B1)		1.5	3.1	4.4	1.5	5	1.5	4.4	
	SEL (B2)		1.6	3.6	5.1	1.6	6.2	1.6	5.9	
t_{PZH}	\overline{OE}	A or B	1	3.3	4.7	1	6.4	1	5.7	ns
t_{PZL}			1.6	3.8	5.1	1.6	6.5	1.6	5.8	
t_{PHZ}	\overline{OE}	A or B	2.2	4.1	5.4	2.2	7.5	2.2	6.4	ns
t_{PLZ}			1.3	3.2	4.4	1.3	5.4	1.3	4.8	



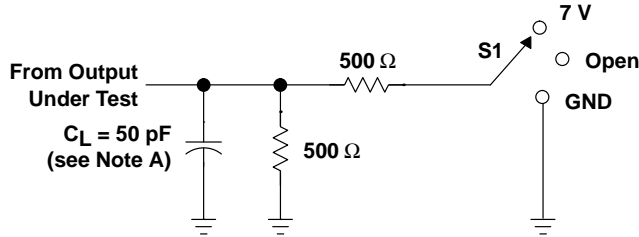
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12-BIT TO 24-BIT MULTIPLEXED D-TYPE LATCHES

WITH 3-STATE OUTPUTS

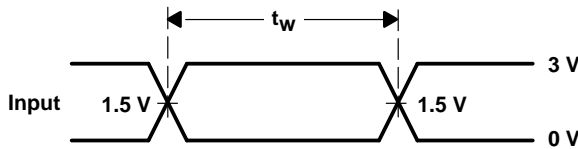
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PARAMETER MEASUREMENT INFORMATION

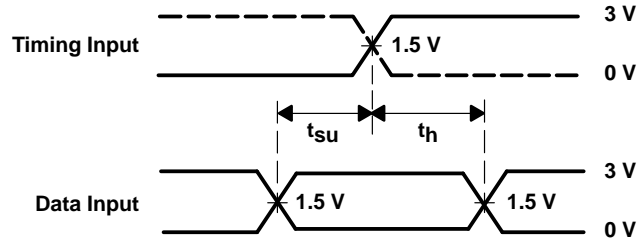


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

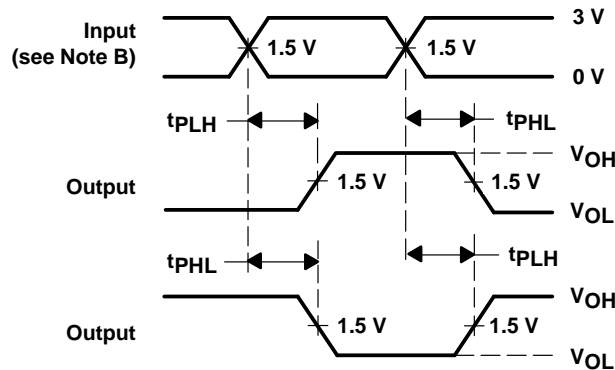
LOAD CIRCUIT FOR OUTPUTS



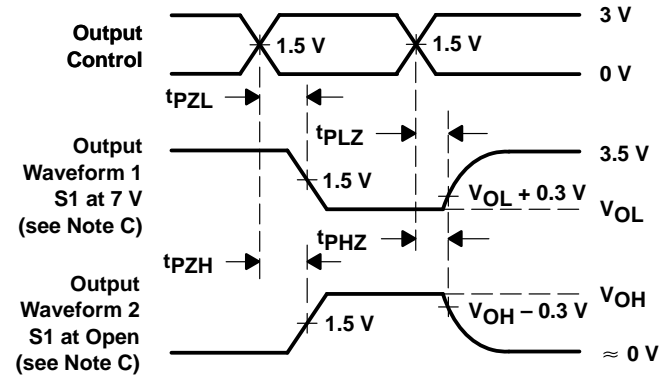
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- C_L includes probe and jig capacitance.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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