

SN54ABT16652, SN74ABT16652 16-BIT BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SCBS215A – FEBRUARY 1991 – REVISED JULY 1994

- Members of the Texas Instruments *Widebus™* Family
- State-of-the-Art *EPIC-II B™* BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce) < 1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- High-Drive Outputs ($-32\text{-mA } I_{OH}$, $64\text{-mA } I_{OL}$)
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) Package and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

description

The 'ABT16652 are 16-bit bus transceivers that consist of D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. These devices can be used as two 8-bit transceivers or one 16-bit transceiver.

Output-enable (OEAB and $\overline{\text{OEBA}}$) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A low input selects real-time data, and a high input selects stored data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'ABT16652.

Data on the A or B data bus, or both, can be stored in the internal D-type flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) inputs regardless of the select- or enable-control pins. When SAB and SBA are in the real-time transfer mode, it is possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and $\overline{\text{OEBA}}$. In this configuration, each output reinforces its input. When all other data sources to the two sets of bus lines are at high impedance, each set of bus lines remains at its last state.

To ensure the high-impedance state during power up or power down, $\overline{\text{OEBA}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver (B to A). OEAB should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver (A to B).

The SN74ABT16652 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

SN54ABT16652 . . . WD PACKAGE
SN74ABT16652 . . . DL PACKAGE
(TOP VIEW)

| | | | |
|----------|----|----|----------|
| 1OEAB | 1 | 56 | 1OEBA |
| 1CLKAB | 2 | 55 | 1CLKBA |
| 1SAB | 3 | 54 | 1SBA |
| GND | 4 | 53 | GND |
| 1A1 | 5 | 52 | 1B1 |
| 1A2 | 6 | 51 | 1B2 |
| V_{CC} | 7 | 50 | V_{CC} |
| 1A3 | 8 | 49 | 1B3 |
| 1A4 | 9 | 48 | 1B4 |
| 1A5 | 10 | 47 | 1B5 |
| GND | 11 | 46 | GND |
| 1A6 | 12 | 45 | 1B6 |
| 1A7 | 13 | 44 | 1B7 |
| 1A8 | 14 | 43 | 1B8 |
| 2A1 | 15 | 42 | 2B1 |
| 2A2 | 16 | 41 | 2B2 |
| 2A3 | 17 | 40 | 2B3 |
| GND | 18 | 39 | GND |
| 2A4 | 19 | 38 | 2B4 |
| 2A5 | 20 | 37 | 2B5 |
| 2A6 | 21 | 36 | 2B6 |
| V_{CC} | 22 | 35 | V_{CC} |
| 2A7 | 23 | 34 | 2B7 |
| 2A8 | 24 | 33 | 2B8 |
| GND | 25 | 32 | GND |
| 2SAB | 26 | 31 | 2SBA |
| 2CLKAB | 27 | 30 | 2CLKBA |
| 2OEAB | 28 | 29 | 2OEBA |

Widebus and EPIC-II B are trademarks of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1994, Texas Instruments Incorporated

SN54ABT16652, SN74ABT16652

16-BIT BUS TRANSCEIVERS AND REGISTERS

WITH 3-STATE OUTPUTS

SCBS215A – FEBRUARY 1991 – REVISED JULY 1994

description (continued)

The SN54ABT16652 is characterized for operation over the full military temperature range of -55°C to 125°C .
The SN74ABT16652 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE

| INPUTS | | | | | | DATA I/O† | | OPERATION OR FUNCTION |
|--------|------|--------|--------|-----|-----|--------------|--------------|---|
| OEAB | OEBA | CLKAB | CLKBA | SAB | SBA | A1 THRU A8 | B1 THRU B8 | |
| L | H | H or L | H or L | X | X | Input | Input | Isolation |
| L | H | ↑ | ↑ | X | X | Input | Input | Store A and B data |
| X | H | ↑ | H or L | X | X | Input | Unspecified‡ | Store A, hold B |
| H | H | ↑ | ↑ | X‡ | X | Input | Output | Store A in both registers |
| L | X | H or L | ↑ | X | X | Unspecified‡ | Input | Hold A, store B |
| L | L | ↑ | ↑ | X | X‡ | Output | Input | Store B in both registers |
| L | L | X | X | X | L | Output | Input | Real-time B data to A bus |
| L | L | X | H or L | X | H | Output | Input | Stored B data to A bus |
| H | H | X | X | L | X | Input | Output | Real-time A data to B bus |
| H | H | H or L | X | H | X | Input | Output | Stored A data to B bus |
| H | L | H or L | H or L | H | H | Output | Output | Stored A data to B bus and stored B data to A bus |

† The data output functions may be enabled or disabled by a variety of level combinations at the OEAB or OEBA inputs. Data input functions are always enabled; i.e., data at the bus pins is stored on every low-to-high transition on the clock inputs.

‡ Select control = L; clocks can occur simultaneously.

Select control = H; clocks must be staggered in order to load both registers.

SN54ABT16652, SN74ABT16652
16-BIT BUS TRANSCEIVERS AND REGISTERS
WITH 3-STATE OUTPUTS

SCBS215A – FEBRUARY 1991 – REVISED JULY 1994

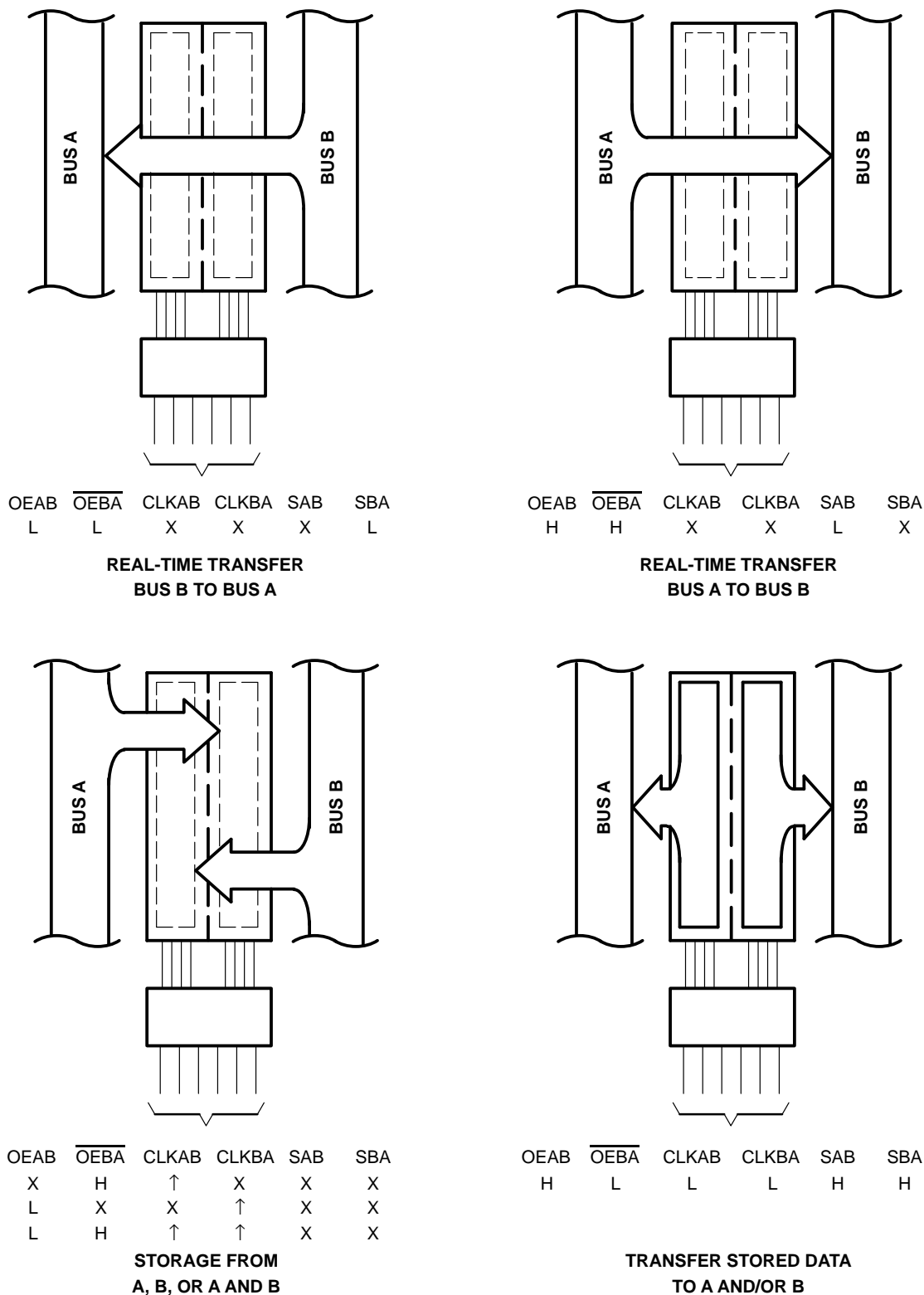


Figure 1. Bus-Management Functions

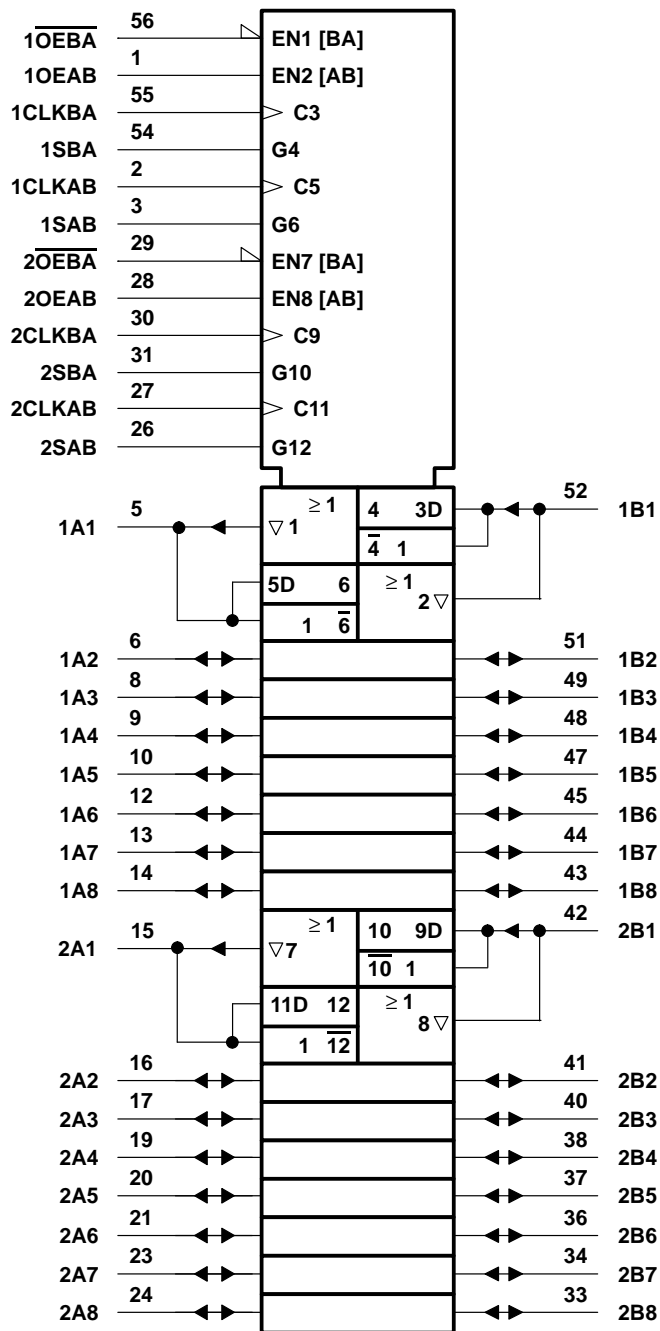
SN54ABT16652, SN74ABT16652

16-BIT BUS TRANSCEIVERS AND REGISTERS

WITH 3-STATE OUTPUTS

SCBS215A – FEBRUARY 1991 – REVISED JULY 1994

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

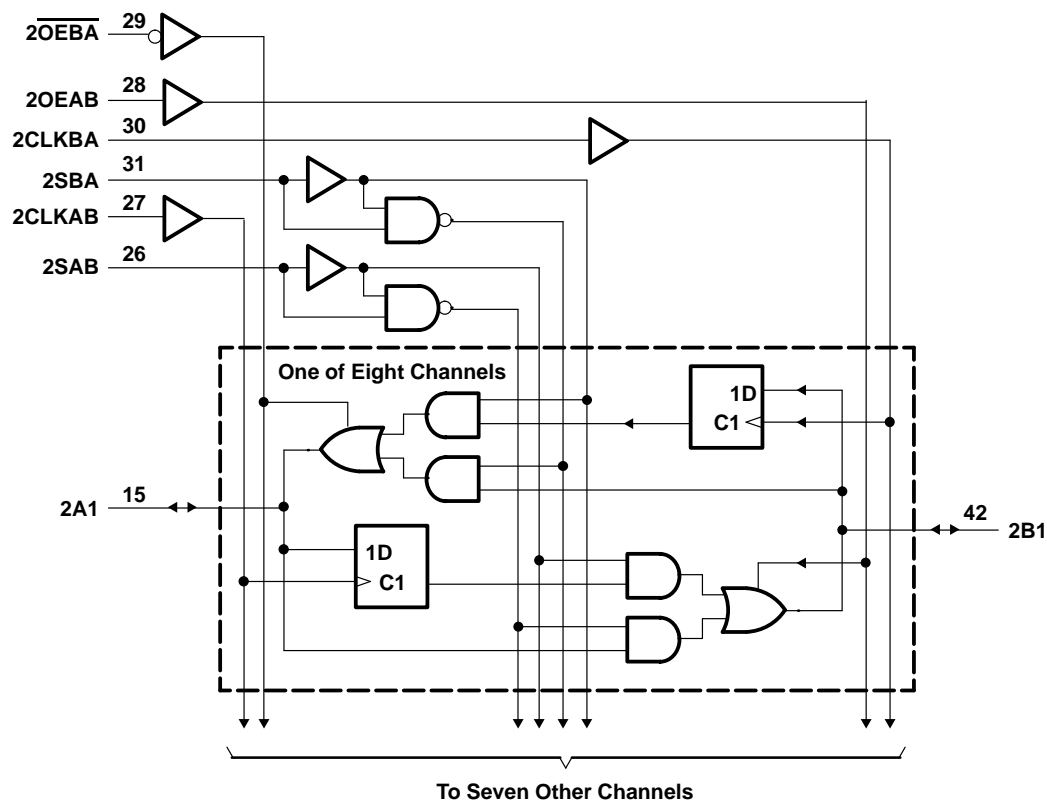
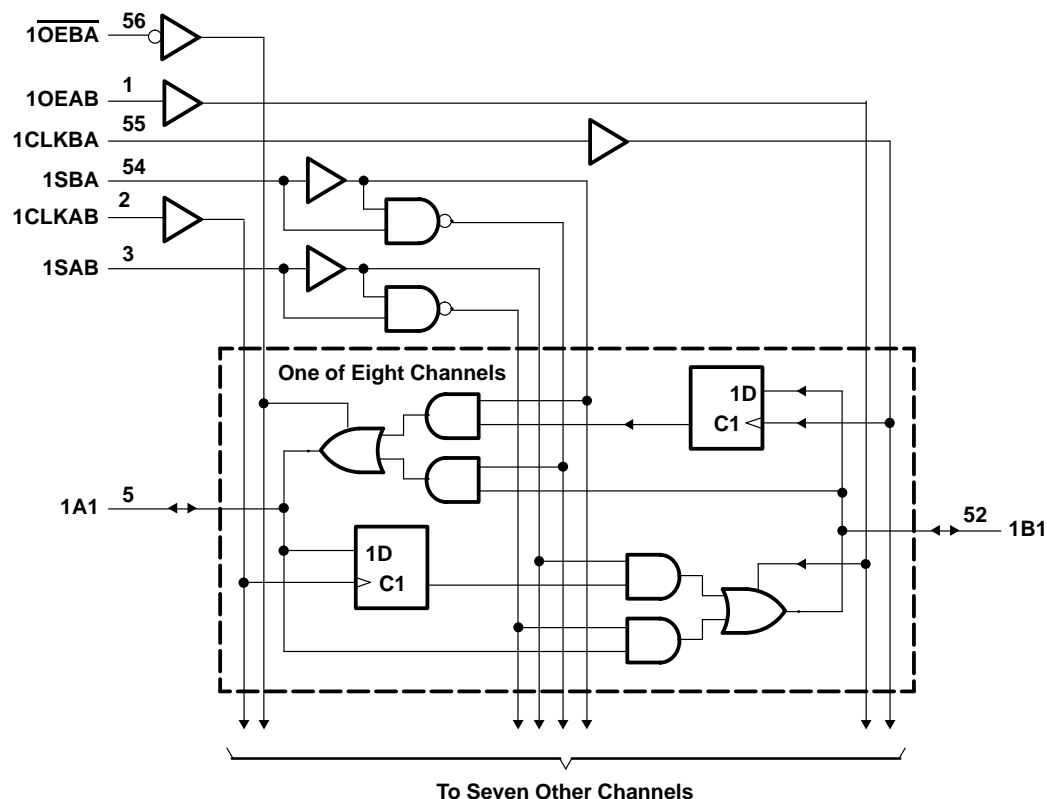


POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN54ABT16652, SN74ABT16652
16-BIT BUS TRANSCEIVERS AND REGISTERS
WITH 3-STATE OUTPUTS

SCBS215A – FEBRUARY 1991 – REVISED JULY 1994

logic diagram (positive logic)



SN54ABT16652, SN74ABT16652

16-BIT BUS TRANSCEIVERS AND REGISTERS

WITH 3-STATE OUTPUTS

SCBS215A – FEBRUARY 1991 – REVISED JULY 1994

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

| | |
|---|-----------------|
| Supply voltage range, V_{CC} | –0.5 V to 7 V |
| Input voltage range, V_I (except I/O ports) (see Note 1) | –0.5 V to 7 V |
| Voltage range applied to any output in the high state or power-off state, V_O | –0.5 V to 5.5 V |
| Current into any output in the low state, I_O : SN54ABT16652 | 96 mA |
| SN74ABT16652 | 128 mA |
| Input clamp current, I_{IK} ($V_I < 0$) | –18 mA |
| Output clamp current, I_{OK} ($V_O < 0$) | –50 mA |
| Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2): DL package | 1.4 W |
| Storage temperature range | –65°C to 150°C |

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 3)

| | | SN54ABT16652 | | SN74ABT16652 | | UNIT |
|---------------------|------------------------------------|-----------------|----------|--------------|----------|------|
| | | MIN | MAX | MIN | MAX | |
| V_{CC} | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| V_{IH} | High-level input voltage | 2 | | 2 | | V |
| V_{IL} | Low-level input voltage | | 0.8 | | 0.8 | V |
| V_I | Input voltage | 0 | V_{CC} | 0 | V_{CC} | V |
| I_{OH} | High-level output current | | –24 | | –32 | mA |
| I_{OL} | Low-level output current | | 48 | | 64 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | Outputs enabled | | | 10 | ns/V |
| T_A | Operating free-air temperature | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused or floating pins (input or I/O) must be held high or low.



SN54ABT16652, SN74ABT16652

16-BIT BUS TRANSCEIVERS AND REGISTERS

WITH 3-STATE OUTPUTS

SCBS215A – FEBRUARY 1991 – REVISED JULY 1994

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | T _A = 25°C | | | SN54ABT16652 | | SN74ABT16652 | | UNIT |
|--------------------|----------------|--|--------------------------|-----------------------|------|-------|--------------|------|--------------|------|------|
| | | | | MIN | TYP† | MAX | MIN | MAX | MIN | MAX | |
| V _{IK} | | V _{CC} = 4.5 V, I _I = -18 mA | | | | -1.2 | | -1.2 | | -1.2 | V |
| V _{OH} | | V _{CC} = 4.5 V, I _{OH} = -3 mA | | 2.5 | | | 2.5 | | 2.5 | | V |
| | | V _{CC} = 5 V, I _{OH} = -3 mA | | 3 | | | 3 | | 3 | | |
| | | V _{CC} = 4.5 V | I _{OH} = -24 mA | 2 | | | 2 | | | | |
| | | | I _{OH} = -32 mA | 2* | | | | | 2 | | |
| V _{OL} | | V _{CC} = 4.5 V | I _{OL} = 48 mA | | | 0.55 | | 0.55 | | | V |
| | | | I _{OL} = 64 mA | | | 0.55* | | | | 0.55 | |
| I _I | Control inputs | V _{CC} = 5.5 V, V _I = V _{CC} or GND | | | | ±1 | | ±1 | | ±1 | μA |
| | A or B ports | V _{CC} = 5.5 V, V _I = V _{CC} or GND | | | | ±20 | | ±20 | | ±20 | |
| I _{OZH} ‡ | | V _{CC} = 5.5 V, V _O = 2.7 V | | | | 10 | | 10 | | 10 | μA |
| I _{OZL} ‡ | | V _{CC} = 5.5 V, V _O = 0.5 V | | | | -10 | | -10 | | -10 | μA |
| I _{off} | | V _{CC} = 0, V _I or V _O ≤ 4.5 V | | | | ±100 | | | | ±100 | μA |
| I _{CEX} | Outputs high | V _{CC} = 5.5 V, V _O = 5.5 V | | | | 50 | | 50 | | 50 | μA |
| I _O § | | V _{CC} = 5.5 V, V _O = 2.5 V | | -50 | -100 | -180 | -50 | -180 | -50 | -180 | mA |
| I _{CC} | A or B ports | V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND | Outputs high | | | 2 | | 2 | | 2 | mA |
| | | | Outputs low | | | 32 | | 32 | | 32 | |
| | | | Outputs disabled | | | 2 | | 2 | | 2 | |
| ΔI _{CC} ¶ | Data inputs | V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND | Outputs enabled | | | 50 | | 50 | | 50 | μA |
| | | | Outputs disabled | | | 50 | | 50 | | 50 | |
| | Control inputs | V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND | | | | 50 | | 50 | | 50 | |
| C _i | Control inputs | V _I = 2.5 V or 0.5 V | | | | 4 | | | | | pF |
| C _{io} | A or B ports | V _O = 2.5 V or 0.5 V | | | | 8 | | | | | pF |

* On products compliant to MIL-STD-883, Class B, this parameter does not apply.

† All typical values are at V_{CC} = 5 V.

‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 2)

| | | V _{CC} = 5 V, T _A = 25°C | | SN54ABT16652 | | SN74ABT16652 | | UNIT |
|--------------------|--|--|-----|--------------|-----|--------------|-----|------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| f _{clock} | Clock frequency | 0 | 125 | 0 | 125 | 0 | 125 | MHz |
| t _w | Pulse duration, CLK high or low | 4.3 | | 4.3 | | 4.3 | | ns |
| t _{su} | Setup time, A or B before CLKAB↑ or CLKBA↑ | 3 | | 4 | | 3 | | ns |
| t _h | Hold time, A or B after CLKAB↑ or CLKBA↑ | 0 | | 0.5 | | 0 | | ns |



SN54ABT16652, SN74ABT16652

16-BIT BUS TRANSCEIVERS AND REGISTERS

WITH 3-STATE OUTPUTS

SCBS215A – FEBRUARY 1991 – REVISED JULY 1994

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 2)

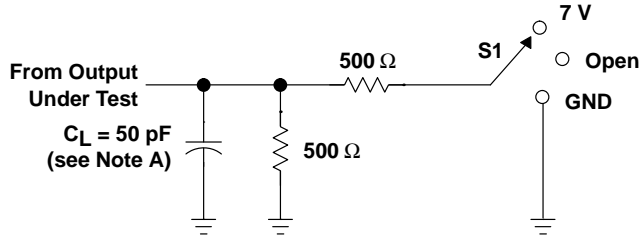
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$ | | | SN54ABT16652 | | SN74ABT16652 | | UNIT |
|------------|-------------------|----------------|---|-----|-----|--------------|-----|--------------|-----|------|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| f_{\max} | | | 125 | | | 125 | | 125 | | MHz |
| t_{PLH} | CLK | B or A | 1.5 | 3.1 | 4 | 1 | 5 | 1.5 | 4.9 | ns |
| t_{PHL} | | | 1.5 | 3.2 | 4.1 | 1 | 5 | 1.5 | 4.7 | |
| t_{PLH} | A or B | B or A | 1 | 2.3 | 3.2 | 0.6 | 4 | 1 | 3.9 | ns |
| t_{PHL} | | | 1 | 3 | 4.1 | 0.6 | 4.9 | 1 | 4.6 | |
| t_{PLH} | SAB or SBA† | B or A | 1 | 2.9 | 4.3 | 0.6 | 5.3 | 1 | 5 | ns |
| t_{PHL} | | | 1 | 3.1 | 4.3 | 0.6 | 5.3 | 1 | 5 | |
| t_{PZH} | \overline{OEBA} | A | 1 | 2.8 | 4.1 | 0.6 | 5.2 | 1 | 5 | ns |
| t_{PZL} | | | 1.5 | 3.1 | 4.4 | 1 | 5.4 | 1.5 | 5.3 | |
| t_{PHZ} | \overline{OEBA} | A | 1.5 | 3.4 | 4.4 | 0.8 | 5.3 | 1.5 | 4.9 | ns |
| t_{PLZ} | | | 1.5 | 2.7 | 3.6 | 1 | 5.3 | 1.5 | 4 | |
| t_{PZH} | OEAB | B | 1 | 2.6 | 3.6 | 0.8 | 4.7 | 1 | 4.2 | ns |
| t_{PZL} | | | 1.5 | 2.8 | 3.9 | 1 | 5 | 1.5 | 4.6 | |
| t_{PHZ} | OEAB | B | 2 | 4.2 | 5.5 | 1 | 6.4 | 2 | 5.9 | ns |
| t_{PLZ} | | | 1.5 | 3.4 | 4.5 | 1 | 5.9 | 1.5 | 5.2 | |

† These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

SN54ABT16652, SN74ABT16652 16-BIT BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

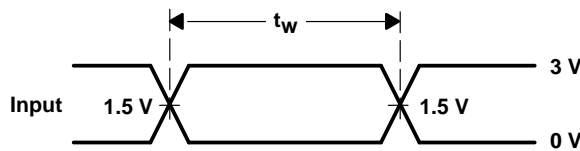
SCBS215A – FEBRUARY 1991 – REVISED JULY 1994

PARAMETER MEASUREMENT INFORMATION

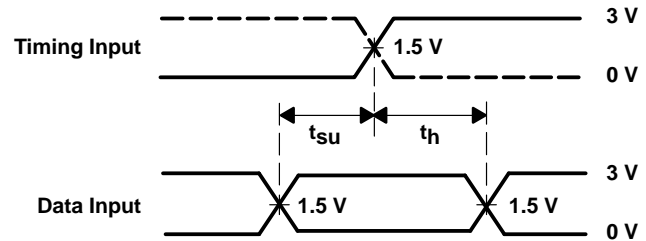


| TEST | S1 |
|-------------------|------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | 7 V |
| t_{PHZ}/t_{PZH} | Open |

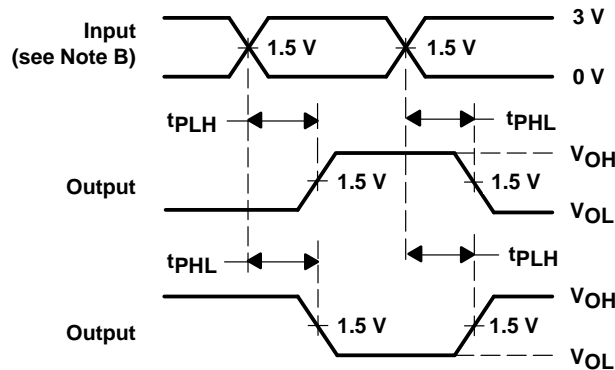
LOAD CIRCUIT FOR OUTPUTS



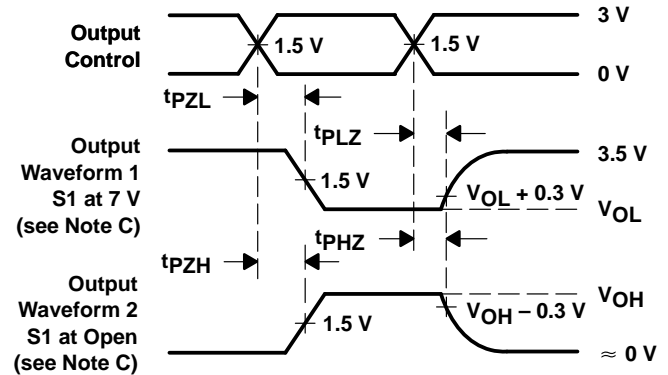
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- C_L includes probe and jig capacitance.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.