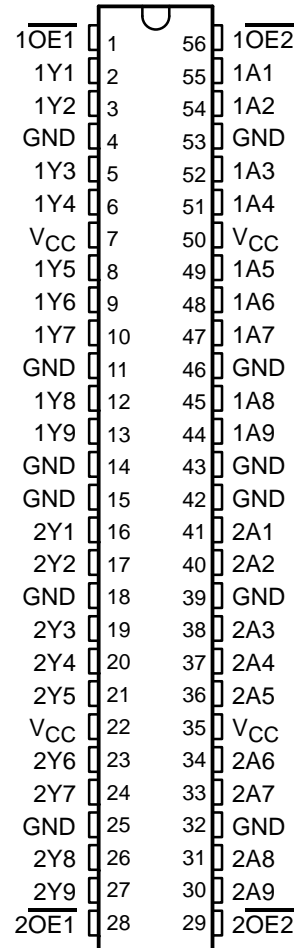


# SN54ABT16825, SN74ABT16825 18-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS218A – JUNE 1992 – REVISED JULY 1994

- Members of the Texas Instruments *Widebus™* Family
- State-of-the-Art *EPIC-II B™* BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical  $V_{OLP}$  (Output Ground Bounce)  $< 1$  V at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$
- Distributed  $V_{CC}$  and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- High-Drive Outputs ( $-32\text{-mA } I_{OH}$ ,  $64\text{-mA } I_{OL}$ )
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

SN54ABT16825 . . . WD PACKAGE  
SN74ABT16825 . . . DGG OR DL PACKAGE  
(TOP VIEW)



## description

The 'ABT16825 are 18-bit buffers and line drivers designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. These devices can be used as two 9-bit buffers or one 18-bit buffer. They provide true data.

The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable ( $\overline{OE1}$  or  $\overline{OE2}$ ) input is high, all nine affected outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT16825 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT16825 is characterized for operation over the full military temperature range of  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ . The SN74ABT16825 is characterized for operation from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .

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# SN54ABT16825, SN74ABT16825

## 18-BIT BUFFERS/DRIVERS

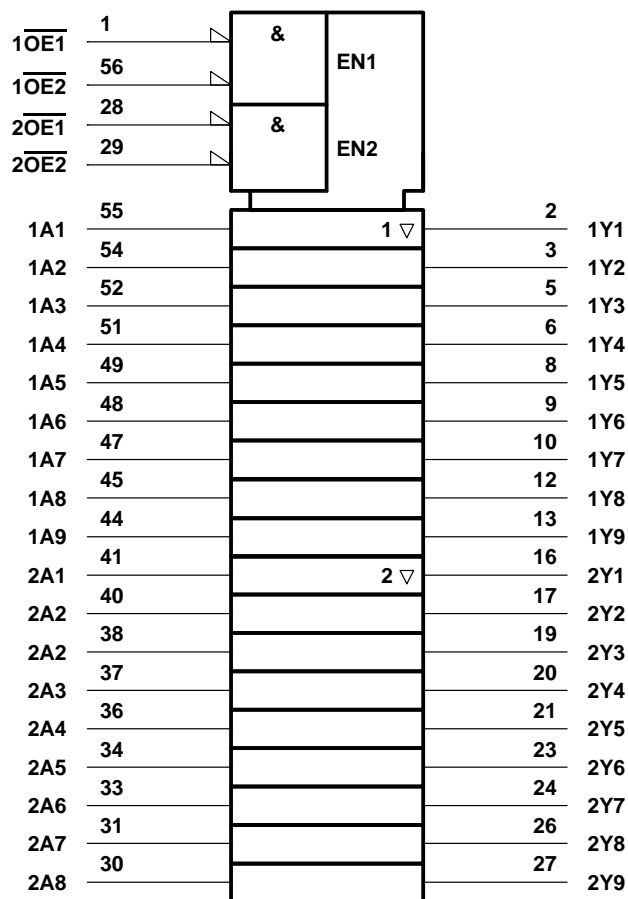
### WITH 3-STATE OUTPUTS

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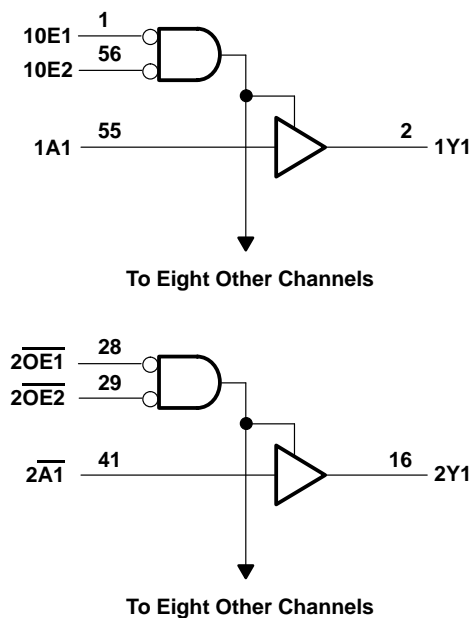
FUNCTION TABLE  
(each 9-bit section)

INPUTS			OUTPUT Y
$\overline{OE1}$	$\overline{OE2}$	A	
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

#### logic symbol†



#### logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

# SN54ABT16825, SN74ABT16825

## 18-BIT BUFFERS/DRIVERS

### WITH 3-STATE OUTPUTS

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#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, $V_O$	–0.5 V to 5.5 V
Current into any output in the low state, $I_O$ : SN54ABT16825	96 mA
SN74ABT16825	128 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–18 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ )	–50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2): DGG package	1 W
DL package	1.4 W
Storage temperature range	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
 2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

#### recommended operating conditions (see Note 3)

			SN54ABT16825		SN74ABT16825		UNIT
			MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage		4.5	5.5	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage		2		2		V
V <sub>IL</sub>	Low-level input voltage			0.8		0.8	V
V <sub>I</sub>	Input voltage		0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current			−24		−32	mA
I <sub>OL</sub>	Low-level output current			48		64	mA
Δt/Δv	Input transition rise or fall rate		Control pins		4		ns/V
			Data pins		10		
Δt/ΔV <sub>CC</sub>	Power-up ramp rate		200		200		μs/V
T <sub>A</sub>	Operating free-air temperature		−55	125	−40	85	°C

NOTE 3: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A = 25^\circ\text{C}$			SN54ABT16825		SN74ABT16825		UNIT
		MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
$V_{IK}$	$V_{CC} = 4.5\text{ V}$ , $I_I = -18\text{ mA}$			-1.2		-1.2		-1.2	V
$V_{OH}$	$V_{CC} = 4.5\text{ V}$ , $I_{OH} = -3\text{ mA}$	2.5			2.5		2.5		V
	$V_{CC} = 5\text{ V}$ , $I_{OH} = -3\text{ mA}$	3			3		3		
	$V_{CC} = 4.5\text{ V}$			2	2				
				2*			2		
$V_{OL}$	$V_{CC} = 4.5\text{ V}$			0.55	0.55				V
				0.55*			0.55		
$I_I$	$V_{CC} = 0\text{ to }5.5\text{ V}$ , $V_I = V_{CC}\text{ or GND}$			$\pm 1$	$\pm 1$		$\pm 1$		$\mu\text{A}$
$I_{OZPU}$	$V_{CC} = 0\text{ to }2.1\text{ V}$ , $V_O = 0.5\text{ to }2.7\text{ V}$ , $\overline{OE} = X$			$\pm 50$	$\pm 50$		$\pm 50$		$\mu\text{A}$
$I_{OZPD}$	$V_{CC} = 2.1\text{ V to }0$ , $V_O = 0.5\text{ to }2.7\text{ V}$ , $\overline{OE} = X$			$\pm 50$	$\pm 50$		$\pm 50$		$\mu\text{A}$
$I_{OZH}$	$V_{CC} = 2.1\text{ V to }5.5\text{ V}$ , $V_O = 2.7\text{ V}$ , $\overline{OE} \geq 2\text{ V}$			10	10		10		$\mu\text{A}$
$I_{OZL}$	$V_{CC} = 2.1\text{ V to }5.5\text{ V}$ , $V_O = 0.5\text{ V}$ , $\overline{OE} \geq 2\text{ V}$			-10	-10		-10		$\mu\text{A}$
$I_{off}$	$V_{CC} = 0$ , $V_I\text{ or }V_O \leq 4.5\text{ V}$			$\pm 100$			$\pm 100$		$\mu\text{A}$
$I_{CEX}$	Outputs high $V_{CC} = 5.5\text{ V}$ , $V_O = 5.5\text{ V}$			50	50		50		$\mu\text{A}$
$I_{O\ddagger}$	$V_{CC} = 5.5\text{ V}$ , $V_O = 2.5\text{ V}$	-50	-100	-180	-50	-180	-50	-180	mA
$I_{CC}$	Outputs high			2	2		2		mA
	Outputs low			32	32		32		
	Outputs disabled $V_I = V_{CC}\text{ or GND}$			2	2		2		
$\Delta I_{CC}\S$	$V_{CC} = 5.5\text{ V}$ , One input at 3.4 V, Other inputs at $V_{CC}\text{ or GND}$			1.5	1.5		1.5		mA
$C_i$	$V_I = 2.5\text{ V or }0.5\text{ V}$								pF
$C_o$	$V_O = 2.5\text{ V or }0.5\text{ V}$								pF

\* On products compliant to MIL-STD-883, Class B, this parameter does not apply.

† All typical values are at  $V_{CC} = 5\text{ V}$ .

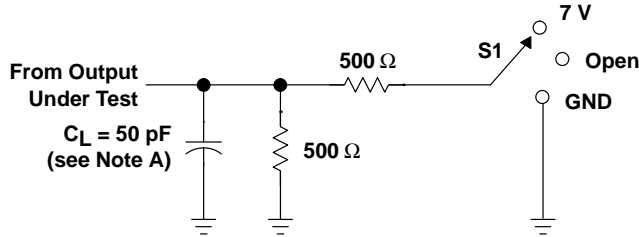
‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50\text{ pF}$  (unless otherwise noted) (see Figure 1)

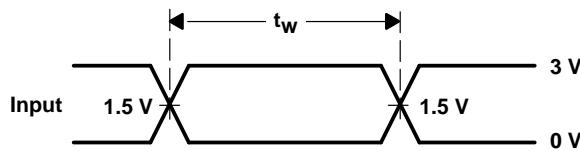
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5\text{ V}$ , $T_A = 25^\circ\text{C}$			SN54ABT16825		SN74ABT16825		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A	Y	1	1.9	3.6	1	4.1	1	3.9	ns
$t_{PHL}$			1	2.1	3.9	1	4.7	1	4.4	
$t_{PZH}$	$\overline{OE}$	Y	1	2.8	5.5	1	6.4	1	6.1	ns
$t_{PZL}$			1	2.8	5.4	1	6.3	1	6	
$t_{PHZ}$	$\overline{OE}$	Y	2.4	4.5	6.8	2.4	7.1	2.4	6.9	ns
$t_{PLZ}$			1.6	3.7	6.2	1.6	7.6	1.6	6.6	

## PARAMETER MEASUREMENT INFORMATION

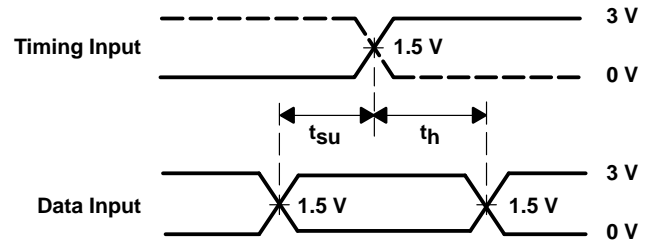


LOAD CIRCUIT FOR OUTPUTS

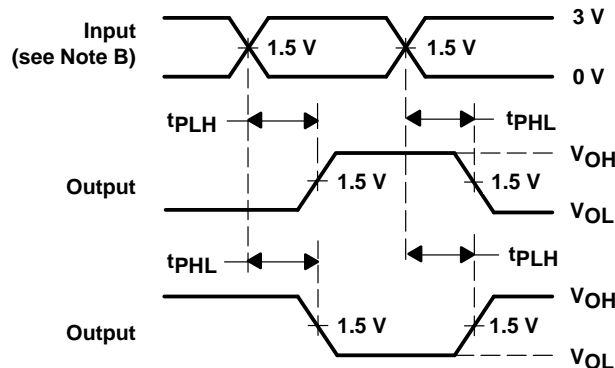
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	7 V
$t_{PHZ}/t_{PZH}$	Open



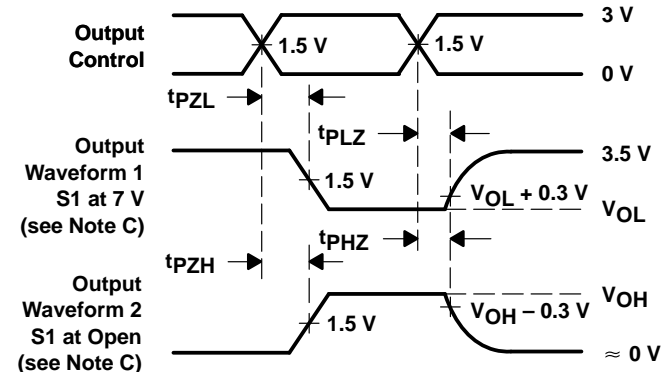
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .  
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



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