

# SN54ABT16841, SN74ABT16841 20-BIT BUS-INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCBS222A – SEPTEMBER 1992 – REVISED JULY 1994

- Members of the Texas Instruments *Widebus™* Family
- State-of-the-Art *EPIC-II B™* BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical  $V_{OLP}$  (Output Ground Bounce) < 0.8 V at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$
- Distributed  $V_{CC}$  and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- High-Drive Outputs (–32-mA  $I_{OH}$ , 64-mA  $I_{OL}$ )
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) Package and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

SN54ABT16841 . . . WD PACKAGE  
SN74ABT16841 . . . DL PACKAGE  
(TOP VIEW)

$\overline{1OE}$	1	56	1LE
1Q1	2	55	1D1
1Q2	3	54	1D2
GND	4	53	GND
1Q3	5	52	1D3
1Q4	6	51	1D4
$V_{CC}$	7	50	$V_{CC}$
1Q5	8	49	1D5
1Q6	9	48	1D6
1Q7	10	47	1D7
GND	11	46	GND
1Q8	12	45	1D8
1Q9	13	44	1D9
1Q10	14	43	1D10
2Q1	15	42	2D1
2Q2	16	41	2D2
2Q3	17	40	2D3
GND	18	39	GND
2Q4	19	38	2D4
2Q5	20	37	2D5
2Q6	21	36	2D6
$V_{CC}$	22	35	$V_{CC}$
2Q7	23	34	2D7
2Q8	24	33	2D8
GND	25	32	GND
2Q9	26	31	2D9
2Q10	27	30	2D10
$\overline{2OE}$	28	29	2LE

## description

These 20-bit latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The 'ABT16841 can be used as two 10-bit latches or one 20-bit latch. The twenty latches are transparent D-type latches. The device has noninverting data (D) inputs and provides true data at its outputs. While the latch-enable (1LE or 2LE) input is high, the Q outputs of the corresponding 10-bit latch follow the D inputs. When LE is taken low, the Q outputs are latched at the levels that were set up at the D inputs.

A buffered output-enable ( $\overline{1OE}$  or  $\overline{2OE}$ ) input can be used to place the outputs of the corresponding 10-bit latch in either a normal logic state (high or low) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly.

The output-enable input does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT16841 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT16841 is characterized for operation over the full military temperature range of  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ . The SN74ABT16841 is characterized for operation from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .

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# SN54ABT16841, SN74ABT16841

## 20-BIT BUS-INTERFACE D-TYPE LATCHES

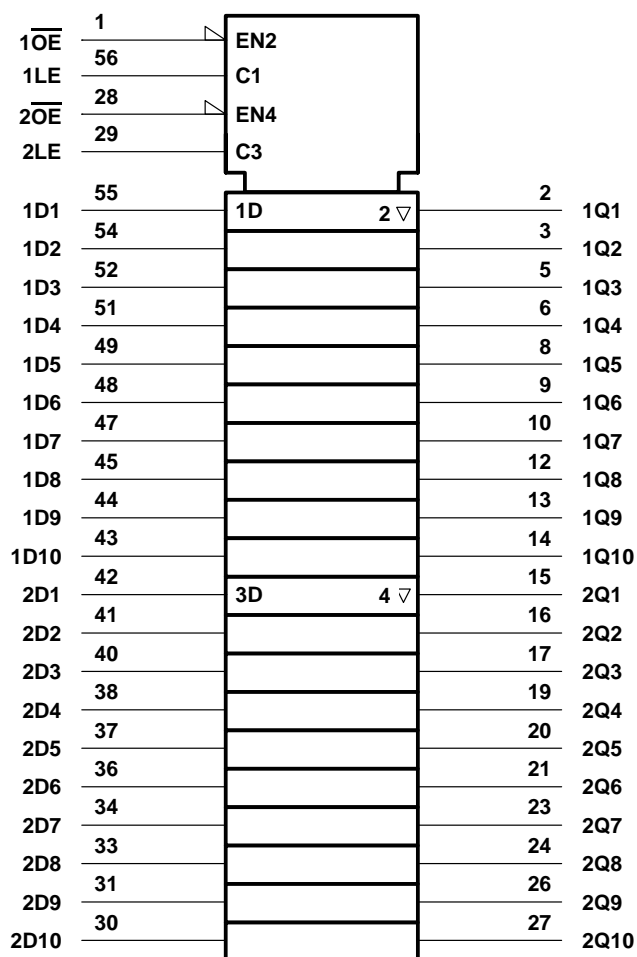
### WITH 3-STATE OUTPUTS

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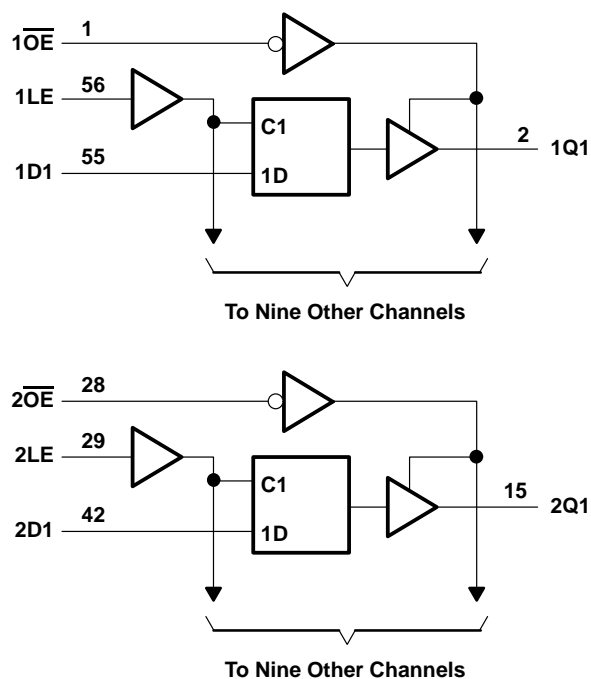
FUNCTION TABLE  
(each 10-bit latch)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	$Q_0$
H	X	X	Z

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, $V_O$	–0.5 V to 5.5 V
Current into any output in the low state, $I_O$ : SN54ABT16841	96 mA
SN74ABT16841	128 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–18 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ )	–50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2): DL package	1.4 W
Storage temperature range	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.  
For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

## recommended operating conditions (see Note 3)

		SN54ABT16841		SN74ABT16841		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	4.5	5.5	4.5	5.5	V
$V_{IH}$	High-level input voltage	2		2		V
$V_{IL}$	Low-level input voltage		0.8		0.8	V
$V_I$	Input voltage	0	$V_{CC}$	0	$V_{CC}$	V
$I_{OH}$	High-level output current		–24		–32	mA
$I_{OL}$	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate				200	μs/V
$T_A$	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused or floating inputs must be held high or low.

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## 20-BIT BUS-INTERFACE D-TYPE LATCHES

### WITH 3-STATE OUTPUTS

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	$T_A = 25^\circ\text{C}$			SN54ABT16841		SN74ABT16841		UNIT
		MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
$V_{IK}$	$V_{CC} = 4.5\text{ V}$ , $I_I = -18\text{ mA}$			-1.2		-1.2		-1.2	V
$V_{OH}$	$V_{CC} = 4.5\text{ V}$ , $I_{OH} = -3\text{ mA}$	2.5			2.5		2.5		V
	$V_{CC} = 5\text{ V}$ , $I_{OH} = -3\text{ mA}$	3			3		3		
	$V_{CC} = 4.5\text{ V}$			2	2				
				2*			2		
$V_{OL}$	$V_{CC} = 4.5\text{ V}$			0.55	0.55				V
				0.55*			0.55		
$I_I$	$V_{CC} = 0\text{ to }5.5\text{ V}$ , $V_I = V_{CC}\text{ or GND}$			$\pm 1$	$\pm 1$		$\pm 1$		$\mu\text{A}$
$I_{OZPU}$	$V_{CC} = 0\text{ to }2.1\text{ V}$ , $V_O = 0.5\text{ to }2.7\text{ V}$ , $\overline{OE} = X$			$\pm 50$	$\pm 50$		$\pm 50$		$\mu\text{A}$
$I_{OZPD}$	$V_{CC} = 2.1\text{ V to }0$ , $V_O = 0.5\text{ to }2.7\text{ V}$ , $\overline{OE} = X$			$\pm 50$	$\pm 50$		$\pm 50$		$\mu\text{A}$
$I_{OZH}$	$V_{CC} = 2.1\text{ V to }5.5\text{ V}$ , $V_O = 2.7\text{ V}$ , $\overline{OE} \geq 2\text{ V}$			10	10		10		$\mu\text{A}$
$I_{OZL}$	$V_{CC} = 2.1\text{ V to }5.5\text{ V}$ , $V_O = 0.5\text{ V}$ , $\overline{OE} \geq 2\text{ V}$			-10	-10		-10		$\mu\text{A}$
$I_{off}$	$V_{CC} = 0$ , $V_I\text{ or }V_O \leq 4.5\text{ V}$			$\pm 100$			$\pm 100$		$\mu\text{A}$
$I_{CEX}$	Outputs high $V_{CC} = 5.5\text{ V}$ , $V_O = 5.5\text{ V}$			50	50		50		$\mu\text{A}$
$I_O^\ddagger$	$V_{CC} = 5.5\text{ V}$ , $V_O = 2.5\text{ V}$	-50	-100	-180	-50	-180	-50	-180	mA
$I_{CC}$	Outputs high			0.5	0.5				mA
	Outputs low			89	89		89		
	Outputs disabled $V_I = V_{CC}\text{ or GND}$			0.5	0.5		0.5		
$\Delta I_{CC}^\S$	$V_{CC} = 5.5\text{ V}$ , One input at 3.4 V, Other inputs at $V_{CC}\text{ or GND}$			1.5	1.5		1.5		mA
$C_i$	$V_I = 2.5\text{ V or }0.5\text{ V}$			3.5					pF
$C_o$	$V_O = 2.5\text{ V or }0.5\text{ V}$			7.5					pF

\* On products compliant to MIL-STD-883, Class B, this parameter does not apply.

† All typical values are at  $V_{CC} = 5\text{ V}$ .

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND.

**timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)**

		$V_{CC} = 5\text{ V}$ , $T_A = 25^\circ\text{C}$		SN54ABT16841		SN74ABT16841		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_w$	Pulse duration, LE high or low	4		4		4		ns
$t_{su}$	Setup time, data before LE↓	1		1		1		ns
$t_h$	Hold time, data after LE↓	2		2		2		ns

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$			SN54ABT16841		SN74ABT16841		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	D	Q	1.1	3.2	4.3	1.1	5.7	1.1	5	ns
$t_{PHL}$			1.6	3.5	4.5	1.6	5.3	1.6	5.1	
$t_{PLH}$	LE	Q	1.1	3.2	4.4	1.1	5.6	1.1	5	ns
$t_{PHL}$			1.6	3.4	4.6	1.6	5.3	1.6	5	
$t_{PZH}$	$\overline{OE}$	Q	1.2	3.2	4.7	1.2	5.8	1.2	5.7	ns
$t_{PZL}$			1.7	3.6	5	1.7	5.7	1.7	5.6	
$t_{PHZ}$	$\overline{OE}$	Q	2.2	4.1	5.7	2.2	6.6	2.2	6.5	ns
$t_{PLZ}$			1.9	4.4	5.8	1.9	8.4	1.9	7.1	

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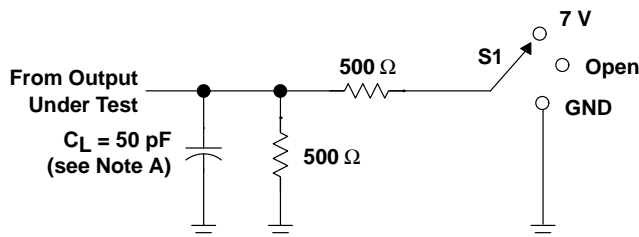
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### WITH 3-STATE OUTPUTS

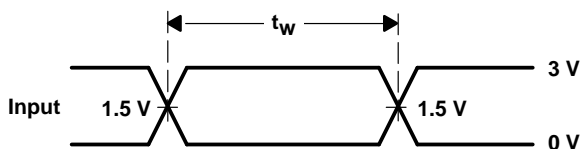
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#### PARAMETER MEASUREMENT INFORMATION

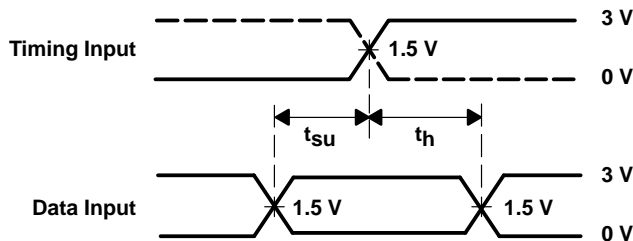


LOAD CIRCUIT FOR OUTPUTS

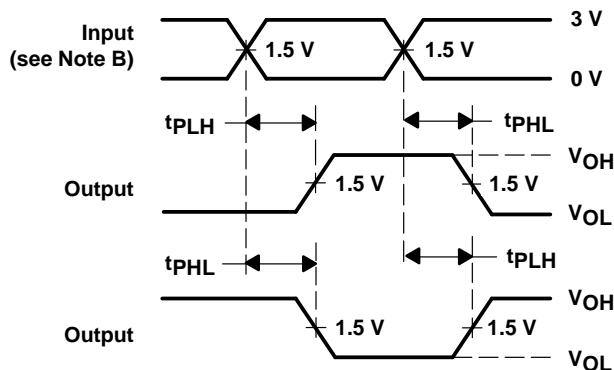
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	7 V
$t_{PHZ}/t_{PZH}$	Open



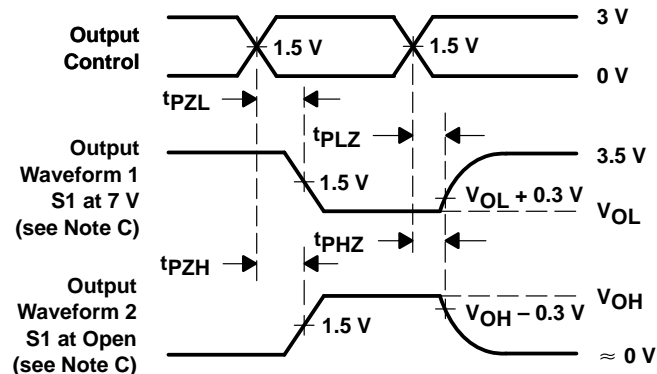
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns.  
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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