

SN54ABT16863, SN74ABT16863 18-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS225A – JUNE 1992 – REVISED JULY 1994

- Members of the Texas Instruments *Widebus™* Family
- State-of-the-Art *EPIC-II B™* BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce) < 1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- High-Drive Outputs ($-32\text{-mA } I_{OH}$, $64\text{-mA } I_{OL}$)
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) Package and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

description

The 'ABT16863 are 18-bit noninverting transceivers designed for asynchronous communication between data buses. The control function implementation minimizes external timing requirements.

The 'ABT16863 can be used as two 9-bit transceivers or one 18-bit transceiver. They allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the output-enable (\overline{OEAB} or \overline{OEBA}) inputs.

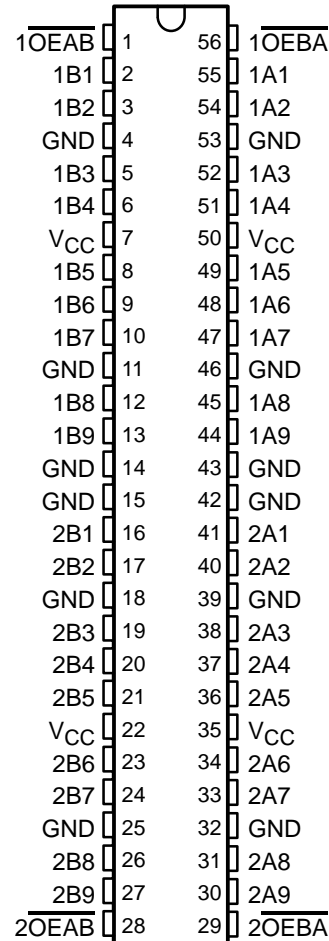
The outputs are in the high-impedance state during power-up and power-down conditions. The outputs remain in the high-impedance state while the device is powered down.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT16863 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT16863 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ABT16863 is characterized for operation from -40°C to 85°C .

SN54ABT16863 . . . WD PACKAGE
SN74ABT16863 . . . DL PACKAGE
(TOP VIEW)



Widebus and EPIC-II B are trademarks of Texas Instruments Incorporated.

UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1994, Texas Instruments Incorporated

SN54ABT16863, SN74ABT16863

18-BIT BUS TRANSCEIVERS

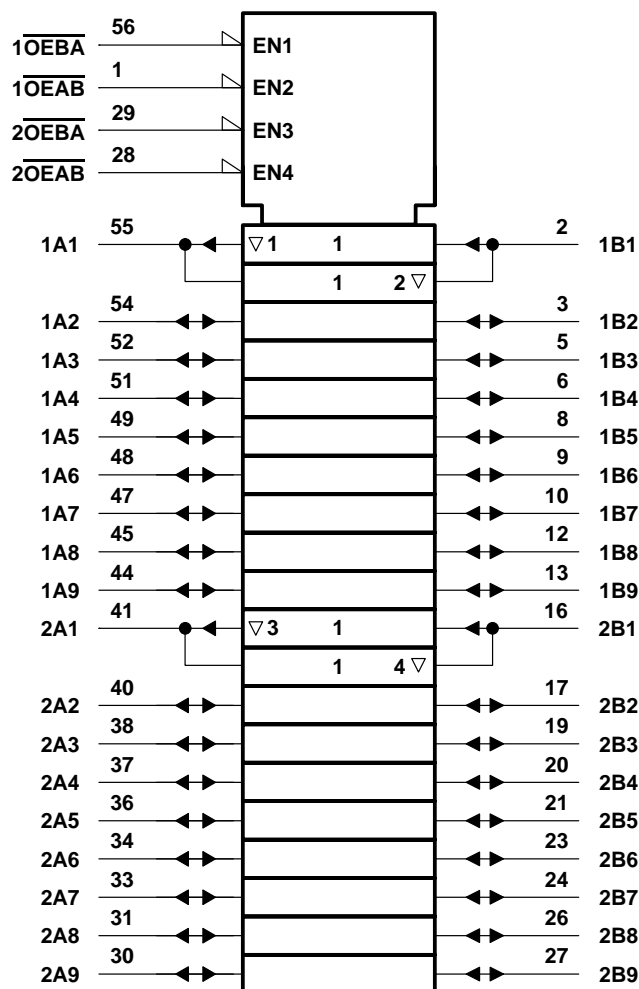
WITH 3-STATE OUTPUTS

SCBS225A – JUNE 1992 – REVISED JULY 1994

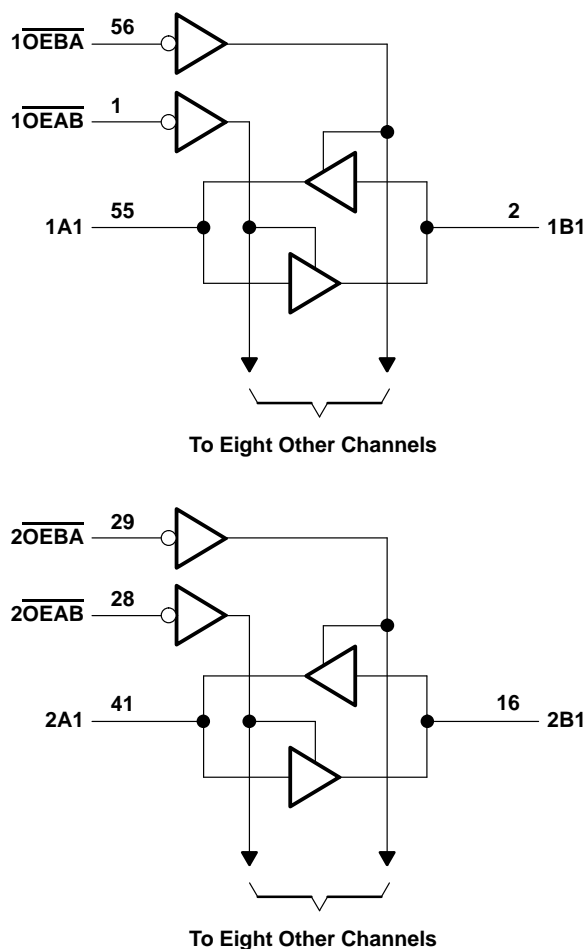
FUNCTION TABLE
(each 9-bit section)

INPUTS		OPERATION
\overline{OEAB}	\overline{OEBA}	
H	L	B data to A bus
L	H	A data to B bus
H	H	Isolation

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN54ABT16863, SN74ABT16863
18-BIT BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

SCBS225A – JUNE 1992 – REVISED JULY 1994

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O	–0.5 V to 5.5 V
Current into any output in the low state, I_O : SN54ABT16863	96 mA
SN74ABT16863	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	–18 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2): DL package	1.4 W
Storage temperature range	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 3)

		SN54ABT16863		SN74ABT16863		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–24		–32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate					μs/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T _A = 25°C			SN54ABT16863		SN74ABT16863		UNIT	
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX		
V _{IK}		V _{CC} = 4.5 V, I _I = –18 mA	–1.2			–1.2		–1.2		V	
V _{OH}		V _{CC} = 4.5 V, I _{OH} = –3 mA	2.5			2.5		2.5		V	
		V _{CC} = 5 V, I _{OH} = –3 mA	3			3		3			
		V _{CC} = 4.5 V	I _{OH} = –24 mA	2			2				
			I _{OH} = –32 mA	2*					2		
V _{OL}		V _{CC} = 4.5 V	I _{OL} = 48 mA			0.55				V	
		I _{OL} = 64 mA	0.55*					0.55			
I _I	Control inputs	V _{CC} = 0 to 5.5 V, V _I = V _{CC} or GND	±1			±1		±1		μA	
	A or B ports	V _{CC} = 2.1 V to 5.5 V, V _I = V _{CC} or GND	±20			±20		±20			
I _{OZPU}		V _{CC} = 0 to 2.1 V, V _O = 0.5 to 2.7 V, $\overline{OE} = X$	±50			±50		±50		μA	
I _{OZPD}		V _{CC} = 2.1 V to 0, V _O = 0.5 to 2.7 V, $\overline{OE} = X$	±50			±50		±50		μA	
I _{OZH} ‡		V _{CC} = 2.1 V to 5.5 V, V _O = 2.7 V, $\overline{OE} \geq 2$ V	10			10		10		μA	
I _{OZL} ‡		V _{CC} = 2.1 V to 5.5 V, V _O = 0.5 V, $\overline{OE} \geq 2$ V	–10			–10		–10		μA	
I _{off}		V _{CC} = 0, V _I or V _O ≤ 4.5 V	±100					±100		μA	
I _{CEX}	Outputs high	V _{CC} = 5.5 V, V _O = 5.5 V	50			50		50		μA	
I _O §		V _{CC} = 5.5 V, V _O = 2.5 V	–50	–100	–180	–50	–180	–50	–180	mA	
I _{CC}	A or B ports	V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND	Outputs high			2		2		mA	
			Outputs low			32		32			
			Outputs disabled			2		2			
ΔI _{CC} ¶	Data inputs	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND	Outputs enabled			1		1.5		mA	
			Outputs disabled			0.05		0.05			
	Control inputs	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND	1.5			1.5		1.5			
C _i	Control inputs	V _I = 2.5 V or 0.5 V	3.5							pF	
C _{io}	A or B ports	V _O = 2.5 V or 0.5 V	9.5							pF	

* On products compliant to MIL-STD-883, Class B, this parameter does not apply.

† All typical values are at V_{CC} = 5 V.

‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

SN54ABT16863, SN74ABT16863
18-BIT BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

SCBS225A – JUNE 1992 – REVISED JULY 1994

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$			SN54ABT16863		SN74ABT16863		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1	2.2	3.2	1	3.7	1	3.5	ns
t_{PHL}			1	2.2	3.4	1	4.2	1	3.9	
t_{PZH}	\overline{OEBA} or \overline{OEAB}	A or B	1	2.9	4.5	1	5.7	1	5.4	ns
t_{PZL}			1	2.6	4.1	1	5.2	1	4.8	
t_{PHZ}	\overline{OEBA} or \overline{OEAB}	A or B	1.6	4.1	5.4	1.6	6.3	1.6	6	ns
t_{PLZ}			1.5	3.3	4.5	1.5	5.3	1.5	5	

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

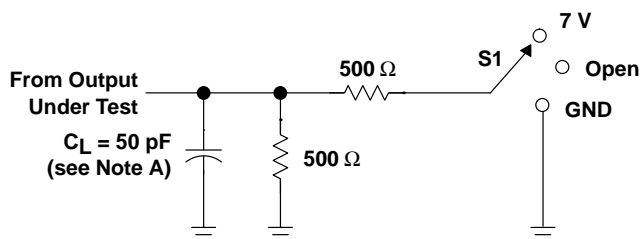
SN54ABT16863, SN74ABT16863

18-BIT BUS TRANSCEIVERS

WITH 3-STATE OUTPUTS

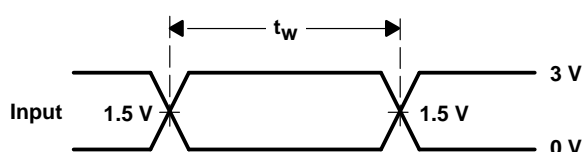
SCBS225A – JUNE 1992 – REVISED JULY 1994

PARAMETER MEASUREMENT INFORMATION

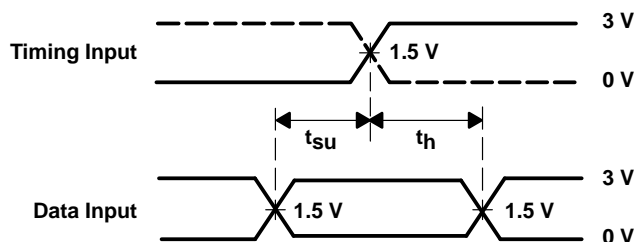


LOAD CIRCUIT FOR OUTPUTS

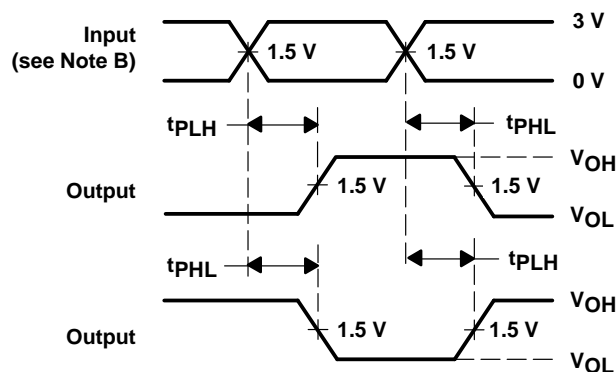
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



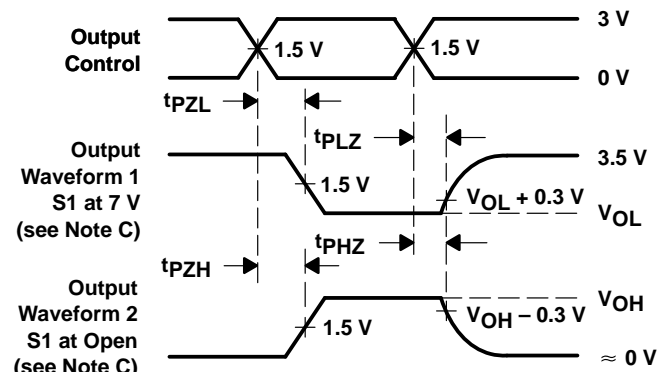
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.