

# SN54ABT2245, SN74ABT2245 OCTAL TRANSCEIVERS AND LINE/MOS DRIVERS WITH 3-STATE OUTPUTS

SCBS234B – SEPTEMBER 1992 – REVISED AUGUST 1994

- B-Port Outputs Have Equivalent 25- $\Omega$  Series Resistors, So No External Resistors Are Required
- State-of-the-Art *EPIC-II B*<sup>™</sup> BiCMOS Design Significantly Reduces Power Dissipation
- Typical  $V_{OLP}$  (Output Ground Bounce) < 1 V at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$
- Package Options Include Plastic Small-Outline (DW) and Shrink Small-Outline (DB) Packages, Ceramic Chip Carriers (FK), and Plastic (N) and Ceramic (J) DIPs

## description

These octal transceivers and line drivers are designed for asynchronous communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The output-enable ( $\overline{OE}$ ) input can be used to disable the device so the buses are effectively isolated.

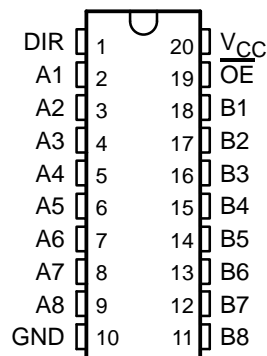
The A-port outputs, which are designed to sink up to 12 mA, include 25- $\Omega$  series resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

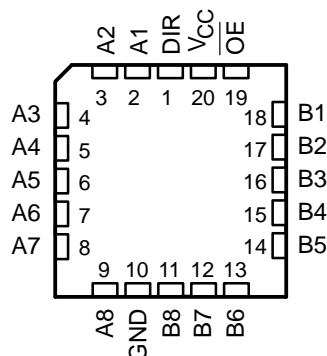
The SN74ABT2245 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54ABT2245 is characterized for operation over the full military temperature range of  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ . The SN74ABT2245 is characterized for operation from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .

SN54ABT2245 . . . J PACKAGE  
SN74ABT2245 . . . DB, DW, OR N PACKAGE  
(TOP VIEW)



SN54ABT2245 . . . FK PACKAGE  
(TOP VIEW)



FUNCTION TABLE

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

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 **TEXAS  
INSTRUMENTS**

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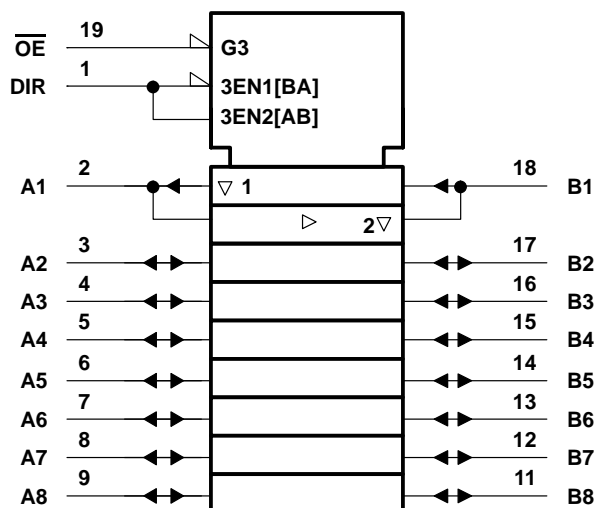
# SN54ABT2245, SN74ABT2245

## OCTAL TRANSCEIVERS AND LINE/MOS DRIVERS

### WITH 3-STATE OUTPUTS

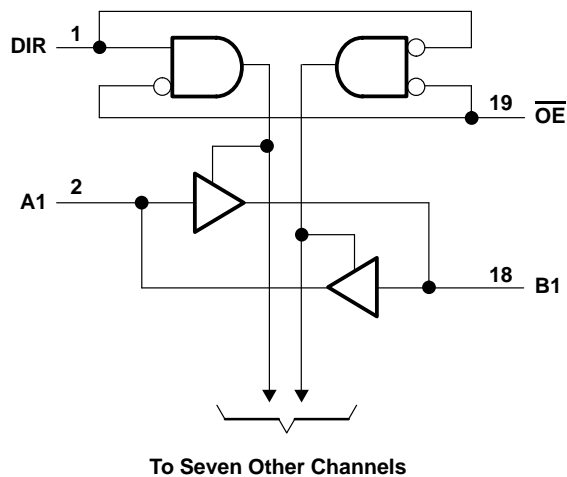
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#### logic symbol†

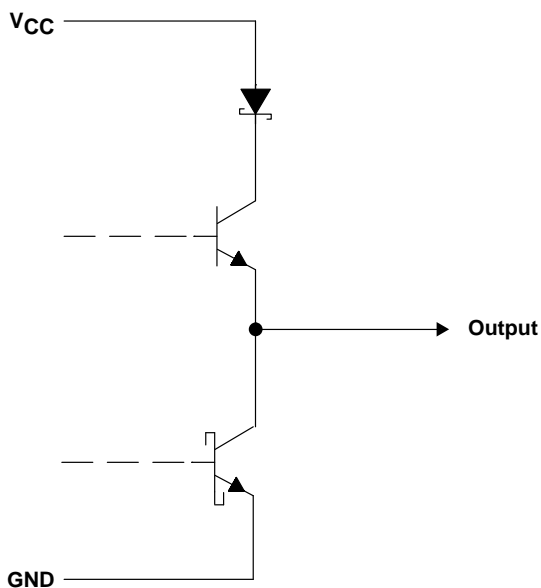


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

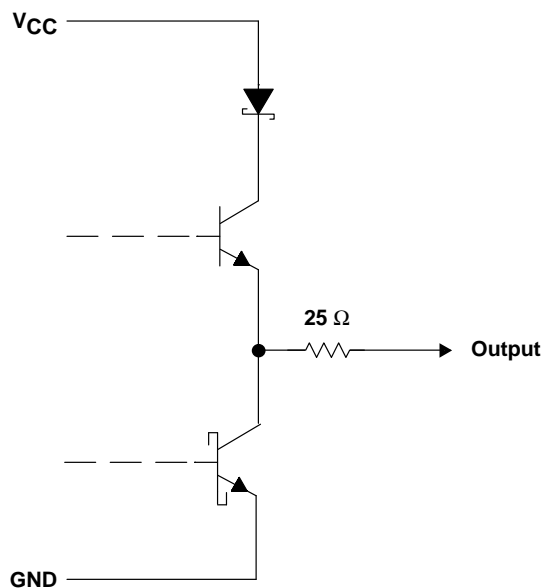
#### logic diagram (positive logic)



#### schematic of A-port outputs



#### schematic of B-port outputs



All resistor values shown are nominal.

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (except I/O ports) (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, $V_O$	–0.5 V to 5.5 V
Current into any output in the low state, $I_O$ : SN54ABT2245 (except B port)	96 mA
SN74ABT2245 (except B port)	128 mA
B port	30 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–18 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ )	–50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2): DB package	0.6 W
DW package	1.6 W
N package	1.3 W
Storage temperature range	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

## recommended operating conditions (see Note 3)

			SN54ABT2245		SN74ABT2245		UNIT
			MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage		4.5	5.5	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage		2		2		V
V <sub>IL</sub>	Low-level input voltage			0.8		0.8	V
V <sub>I</sub>	Input voltage		0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current			−24		−32	mA
I <sub>OL</sub>	Low-level output current		A port		64		mA
			B port		12		
Δt/Δv	Input transition rise or fall rate		Outputs enabled		5		ns/V
Δt/ΔV <sub>CC</sub>	Power-up ramp rate		200		200		μs/V
T <sub>A</sub>	Operating free-air temperature		−55	125	−40	85	°C

NOTE 3: Unused or floating pins (input or I/O) must be held high or low.

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## OCTAL TRANSCEIVERS AND LINE/MOS DRIVERS

### WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TA = 25°C			SN54ABT2245		SN74ABT2245		UNIT		
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX			
VIK		VCC = 4.5 V, II = -18 mA		-1.2			-1.2		-1.2		V		
VOH	B port	VCC = 4.5 V, IOH = -1 mA		3.35			3.3		3.35		V		
		VCC = 5 V, IOH = -1 mA		3.85			3.8		3.85				
		VCC = 4.5 V	IOH = -3 mA					3		3.1			
			IOH = -12 mA		2.6					2.6			
	A port	VCC = 4.5 V, IOH = -3 mA		2.5			2.5		2.5				
		VCC = 5 V, IOH = -3 mA		3			3		3				
		VCC = 4.5 V	IOH = -24 mA		2			2					
			IOH = -32 mA		2*					2			
VOL	B port	VCC = 4.5 V	IOL = 8 mA		0.65		0.8		0.65		V		
			IOL = 12 mA		0.8				0.8				
	A port		IOL = 48 mA		0.55		0.55						
			IOL = 64 mA		0.55*				0.55				
II	Control inputs	VCC = 0 to 5.5 V, VI = VCC or GND		±1			±1		±1		μA		
	A or B ports	VCC = 2.1 V to 5.5 V, VI = VCC or GND		±20			±20		±20				
IOZH‡		VCC = 2.1 V to 5.5 V, VO = 2.7 V, OE ≥ 2 V		10			10		10		μA		
IOZL‡		VCC = 2.1 V to 5.5 V, VO = 0.5 V, OE ≥ 2 V		-10			-10		-10		μA		
IOZPU§		VCC = 0 to 2.1 V, VO = 0.5 V to 2.7 V, OE = X		± 50			± 50		± 50		μA		
IOZPD§		VCC = 2.1 V to 0, VO = 0.5 V to 2.7 V, OE = X		± 50			± 50		± 50		μA		
Ioff		VCC = 0, VI or VO ≤ 4.5 V		±100					±100		μA		
ICEX	Outputs high	VCC = 5.5 V, VO = 5.5 V		50			50		50		μA		
IO¶	B port	VCC = 5.5 V, VO = 2.5 V		-25	-100		-25	-100		-25	-100		mA
	A port			-50	-100 -180		-50	-180		-50	-180		
ICC	A or B ports	VCC = 5.5 V, IO = 0, VI = VCC or GND	Outputs high		1	250		250		250		μA	
			Outputs low		24	32		32		32		mA	
			Outputs disabled		0.5	250		250		250		μA	
ΔICC#	Data inputs	VCC = 5.5 V, One input at 3.4 V, Other inputs at VCC or GND	Outputs enabled		1.5		1.5		1.5		mA		
			Outputs disabled		0.05		0.05		0.05				
	Control inputs	VCC = 5.5 V, One input at 3.4 V, Other inputs at VCC or GND		1.5			1.5		1.5				
Ci		VI = 2.5 V or 0.5 V		3							pF		
Cio		VO = 2.5 V or 0.5 V		6							pF		

\* On products compliant to MIL-STD-883, Class B, this parameter does not apply.

† All typical values are at V<sub>CC</sub> = 5 V.

‡ The parameters I<sub>OZH</sub> and I<sub>OZL</sub> include the input leakage current.

§ This parameter is characterized but not tested.

¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$			SN54ABT2245		SN74ABT2245		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A	B	1	2.5	3.4	1	4	1	3.8	ns
$t_{PHL}$			1	3.2	4.2	1	4.6	1	4.5	
$t_{PLH}$	B	A	1	2.2	3.2	1	3.8	1	3.6	ns
$t_{PHL}$			1	2.7	3.6	1	4.2	1	4	
$t_{PZH}$	$\overline{OE}$	A	1	3.3	4.6	1	5.6	1	5.5	ns
$t_{PZL}$			1	3.2	4.7	1	6	1	5.7	
$t_{PHZ}$	$\overline{OE}$	A	2	4	5.1	2	5.7	2	5.6	ns
$t_{PLZ}$			1	2.9	4	1	4.6	1	4.5	
$t_{PZH}$	$\overline{OE}$	B	1.5	3.6	4.9	1.5	6.3	1.5	6.1	ns
$t_{PZL}$			1.5	3.9	5.3	1.5	6.6	1.5	6.3	
$t_{PHZ}$	$\overline{OE}$	B	1.5	3.6	4.7	1.5	5.5	1.5	5.3	ns
$t_{PLZ}$			1.5	3.3	4.4	1.5	4.9	1.5	4.8	

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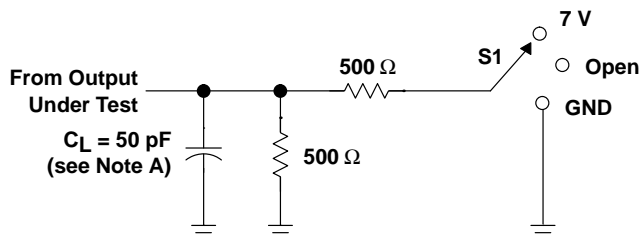
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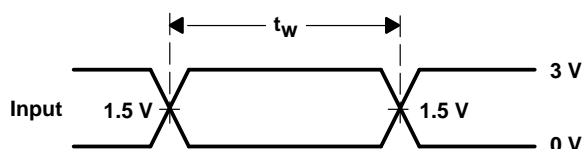
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#### PARAMETER MEASUREMENT INFORMATION

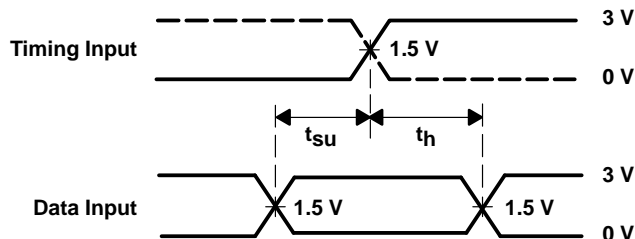


LOAD CIRCUIT FOR OUTPUTS

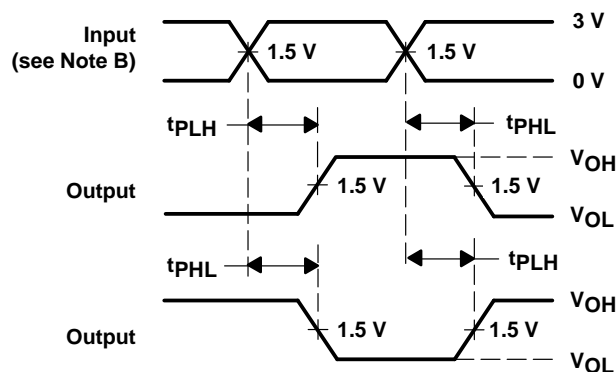
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	7 V
$t_{PHZ}/t_{PZH}$	Open



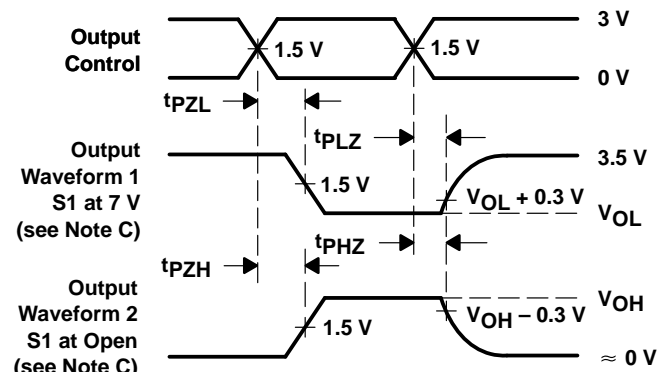
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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