

SN54ABT162500, SN74ABT162500 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS242B – JUNE 1992 – REVISED JULY 1994

- B-Port Outputs Have Equivalent 25- Ω Series Resistors, So No External Resistors Are Required
- Members of the Texas Instruments *Widebus*™ Family
- State-of-the-Art *EPIC-II B*™ BiCMOS Design Significantly Reduces Power Dissipation
- *UBT*™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- Flow-Through Architecture Optimizes PCB Layout
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) Package and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

description

These 18-bit universal bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes. Data flow in each direction is controlled by output-enable ($\overline{\text{OEAB}}$ and $\overline{\text{OEBA}}$), latch-enable ($\overline{\text{LEAB}}$ and $\overline{\text{LEBA}}$), and clock ($\overline{\text{CLKAB}}$ and $\overline{\text{CLKBA}}$) inputs.

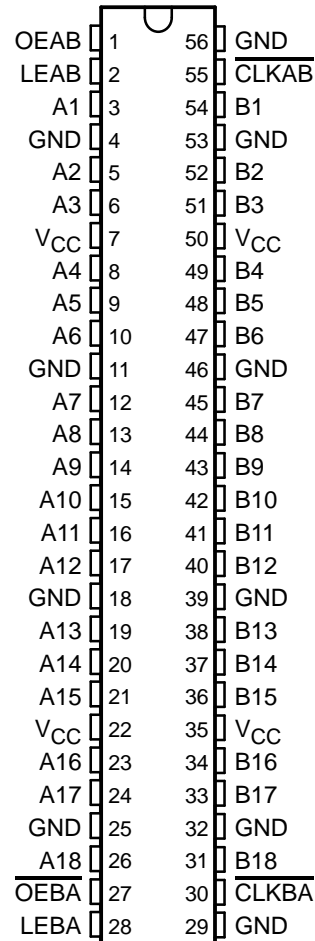
For A-to-B data flow, the device operates in the transparent mode when $\overline{\text{LEAB}}$ is high. When $\overline{\text{LEAB}}$ is low, the A data is latched if $\overline{\text{CLKAB}}$ is held at a high or low logic level. If $\overline{\text{LEAB}}$ is low, the A bus data is stored in the latch/flip-flop on the high-to-low transition of $\overline{\text{CLKAB}}$. Output-enable $\overline{\text{OEAB}}$ is active high. When $\overline{\text{OEAB}}$ is high, the outputs are active. When $\overline{\text{OEAB}}$ is low, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses $\overline{\text{OEBA}}$, $\overline{\text{LEBA}}$, and $\overline{\text{CLKBA}}$. The output enables are complementary ($\overline{\text{OEAB}}$ is active high and $\overline{\text{OEBA}}$ is active low).

The B-port outputs, which are designed to source or sink up to 12 mA, include 25- Ω series resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

SN54ABT162500 . . . WD PACKAGE
SN74ABT162500 . . . DL PACKAGE
(TOP VIEW)



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description (continued)

The SN74ABT162500 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT162500 is characterized over the full military temperature range of -55°C to 125°C . The SN74ABT162500 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE†

INPUTS				OUTPUT
OEAB	LEAB	CLKAB	A	B
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↓	L	L
H	L	↓	H	H
H	L	H	X	B ₀ ‡
H	L	L	X	B ₀ §

† A-to-B data flow is shown: B-to-A flow is similar but uses $\overline{\text{OEBA}}$, $\overline{\text{LEBA}}$, and $\overline{\text{CLKBA}}$.

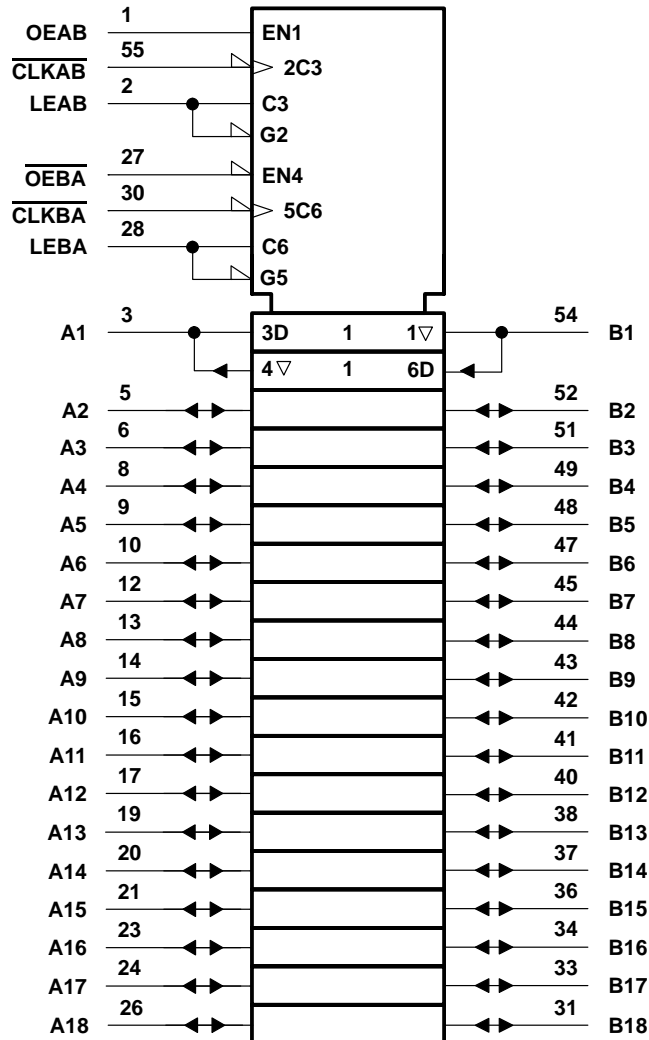
‡ Output level before the indicated steady-state input conditions were established.

§ Output level before the indicated steady-state input conditions were established, provided that $\overline{\text{CLKAB}}$ was low before LEAB went low.

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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

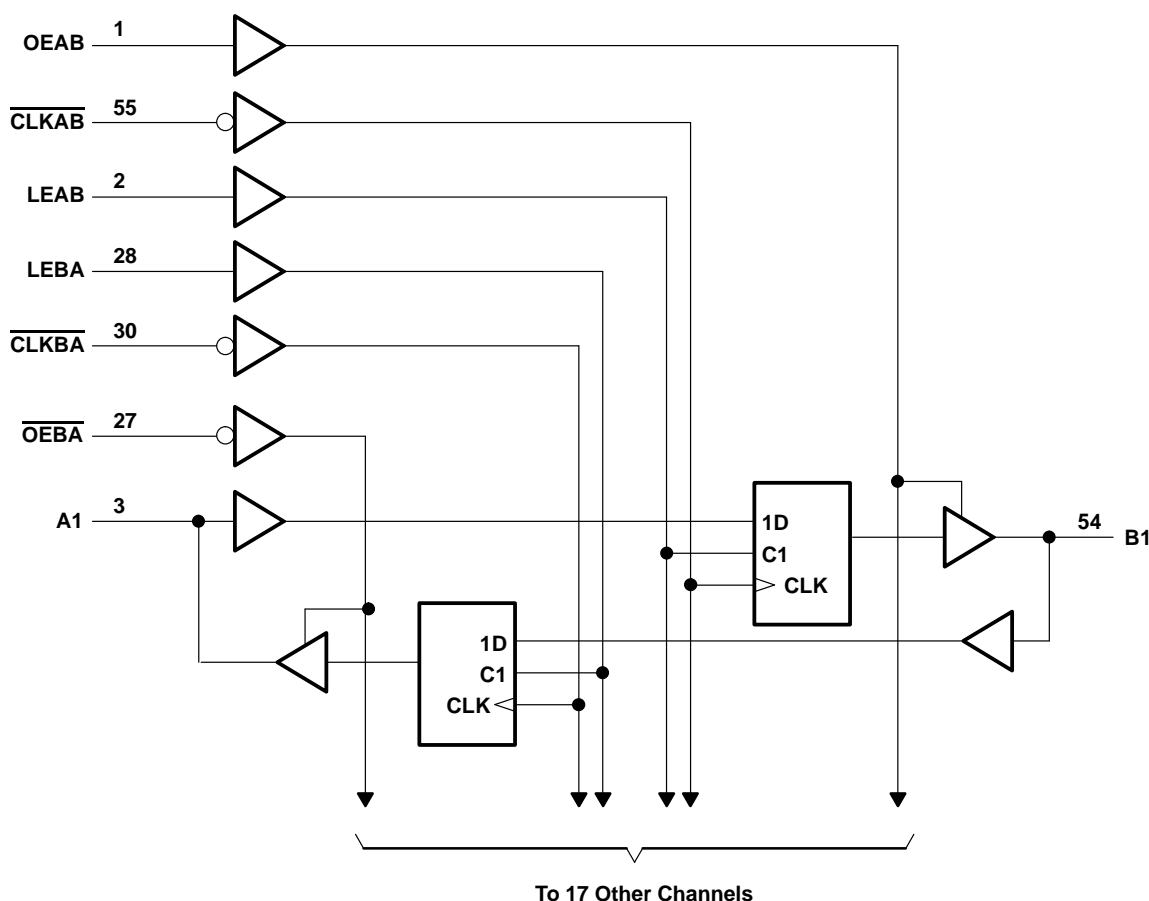
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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O	–0.5 V to 5.5 V
Current into any output in the low state, I_O : SN54ABT162500 (A port)	96 mA
SN74ABT162500 (A port)	128 mA
B port	30 mA
Input clamp current, I_{IK} ($V_I < 0$)	–18 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2): DL package	1.4 W
Storage temperature range	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

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recommended operating conditions (see Note 3)

			SN54ABT162500		SN74ABT162500		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	A port		–24		–32	mA
		B port		–12		–12	
I_{OL}	Low-level output current	A port		48		64	mA
		B port		12		12	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		200		200		$\mu s/V$
T_A	Operating free-air temperature		–55	125	–40	85	$^{\circ}C$

NOTE 3: Unused or floating pins (input or I/O) must be held high or low.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T _A = 25°C			SN54ABT162500		SN74ABT162500		UNIT	
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX		
V _{IK}		V _{CC} = 4.5 V, I _I = −18 mA	−1.2			−1.2		−1.2		V	
V _{OH}	A port	V _{CC} = 4.5 V, I _{OH} = −3 mA	2.5			2.5		2.5		V	
		V _{CC} = 5 V, I _{OH} = −3 mA	3			3		3			
		V _{CC} = 4.5 V	I _{OH} = −24 mA	2			2				
			I _{OH} = −32 mA	2*					2		
	B port	V _{CC} = 4.5 V, I _{OH} = −1 mA	3.35			3.3		3.35			
		V _{CC} = 5 V, I _{OH} = −1 mA	3.85			3.8		3.85			
		V _{CC} = 4.5 V	I _{OH} = −3 mA	3.1			3		3.1		
			I _{OH} = −12 mA	2.6					2.6		
V _{OL}	A port	V _{CC} = 4.5 V	I _{OL} = 48 mA	0.55			0.55		V		
	I _{OL} = 64 mA		0.55*			0.55					
	B port	V _{CC} = 4.5 V, I _{OL} = 12 mA	0.8			0.8		0.8			
I _I	Control inputs	V _{CC} = 0 to 5.5 V, V _I = V _{CC} or GND		±1			±1		±1		
	A or B ports	V _{CC} = 2.1 V to 5.5 V, V _I = V _{CC} or GND		±20			±20		±20		
I _{OZPU}		V _{CC} = 0 to 2.1 V, V _O = 0.5 V to 2.7 V, $\overline{\text{OE}}$ or OE = X		±50			±50		±50		
I _{OZPD}		V _{CC} = 2.1 V to 0, V _O = 0.5 V to 2.7 V, $\overline{\text{OE}}$ or OE = X		±50			±50		±50		
I _{OZH} ‡		V _{CC} = 2.1 V to 5.5 V, V _O = 2.7 V, $\overline{\text{OE}} \geq 2$ V or OE ≤ 0.8 V§		10			10		10		
I _{OZL} ‡		V _{CC} = 2.1 V to 5.5 V, V _O = 0.5 V, $\overline{\text{OE}} \geq 2$ V or OE ≤ 0.8 V§		−10			−10		−10		
I _{off}		V _{CC} = 0, V _I or V _O ≤ 4.5 V		±100					±100		
I _{CEX}	Outputs high	V _{CC} = 5.5 V, V _O = 5.5 V		50			50		50		
I _O ¶	A port	V _{CC} = 5.5 V, V _O = 2.5 V		−50	−110	−180	−50	−180	−50	−180	
	B port	V _{CC} = 5.5 V, V _O = 2.5 V		−25	−55	−90	−25	−90	−25	−90	
I _{CC}	A or B ports	V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND	Outputs high		3			3		3	
			Outputs low		36			36		36	
			Outputs disabled		3			3		3	
ΔI _{CC} #		V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND		50			50		50		
C _i	Control inputs	V _I = 2.5 V or 0.5 V		3							
C _{io}	A or B ports	V _O = 2.5 V or 0.5 V		9							

* On products compliant to MIL-STD-883, Class B, this parameter does not apply.

† All typical values are at V_{CC} = 5 V.

‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.

§ For V_{CC} between 2.1 V and 4 V, OE should be less than or equal to 0.5 V to ensure a low state.

¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

				SN54ABT162500		SN74ABT162500		UNIT
				MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency			0	150	0	150	MHz
t _w	Pulse duration	LEAB or LEBA high		2.5		2.5		ns
		CLKAB or CLKBA high or low		3		3		
t _{su}	Setup time	A before CLKAB↓		3.3		3.3		ns
		B before CLKBA↓		3.3		3.3		
		A before LEAB↓ or B before LEBA↓	CLK high	1		1		
			CLK low	2.5		2.5		
t _h	Hold time	A after CLKAB↓ or B after CLKBA↓		0		0		ns
		A after LEAB↓ or B after LEBA↓		2		2		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$			SN54ABT162500		SN74ABT162500		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			150	200		150		150		MHz
t_{PLH}	A or B	B or A	1.5	2.6	4	1.5	5.1	1.5	4.8	ns
t_{PHL}			2	3.4	5.2	2	6.1	2	5.7	
t_{PLH}	LEAB or LEBA	B or A	2	3.3	4.8	2	6.1	2	5.6	ns
t_{PHL}			2	3.8	5.2	2	6.4	2	5.9	
t_{PLH}	$\overline{\text{CLKAB}}$ or $\overline{\text{CLKBA}}$	B or A	1.5	3.7	4.9	1.5	6.4	1.5	5.9	ns
t_{PHL}			1.5	3.8	5.2	1.5	6.4	1.5	6	
t_{PZH}	OEAB or $\overline{\text{OEBA}}$	B or A	1.5	3.4	4.6	1.5	5.6	1.5	5.3	ns
t_{PZL}			2	3.8	4.7	2	5.6	2	5.4	
t_{PHZ}	OEAB or $\overline{\text{OEBA}}$	B or A	2	4.5	5.7	2	6.9	2	6.5	ns
t_{PLZ}			1.5	3.8	5.3	1.5	6.3	1.5	5.8	

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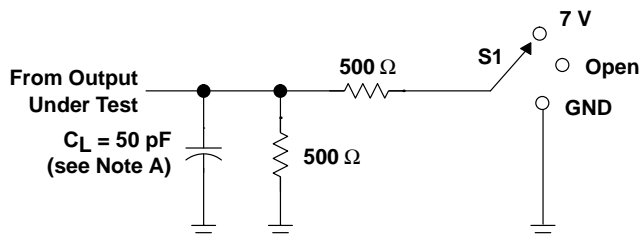
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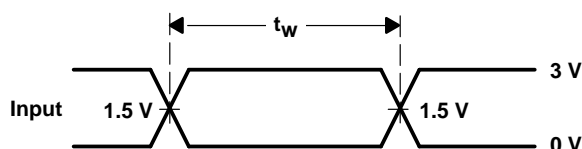
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PARAMETER MEASUREMENT INFORMATION

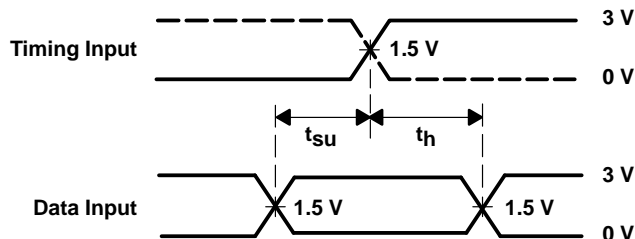


LOAD CIRCUIT FOR OUTPUTS

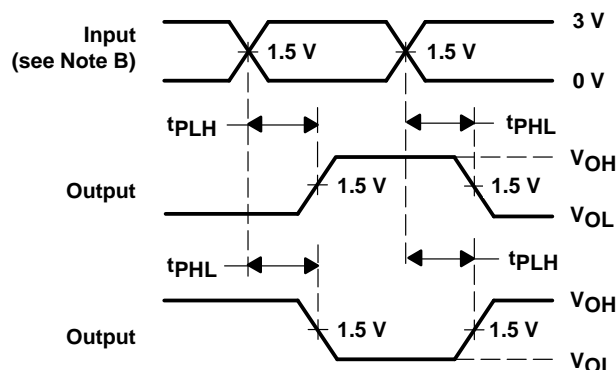
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



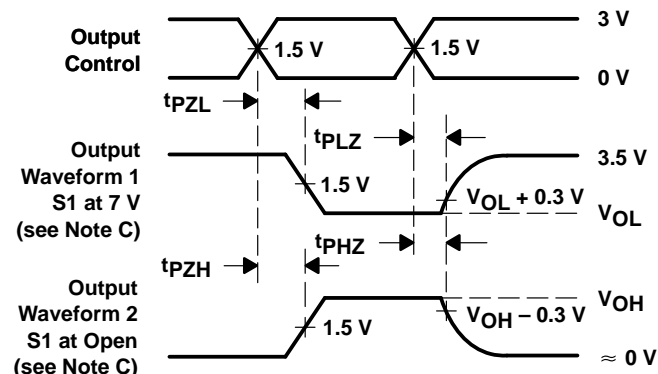
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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