

# SN54ABT162501, SN74ABT162501 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS243B – SEPTEMBER 1992 – REVISED JULY 1994

- B-Port Outputs Have Equivalent 25- $\Omega$  Series Resistors, So No External Resistors Are Required
- Members of the Texas Instruments *Widebus*™ Family
- State-of-the-Art *EPIC-II B*™ BiCMOS Design Significantly Reduces Power Dissipation
- *UBT*™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical  $V_{OLP}$  (Output Ground Bounce) < 0.8 V at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$
- Flow-Through Architecture Optimizes PCB Layout
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

## description

These 18-bit universal bus transceivers consist of storage elements that can operate either as D-type latches or D-type flip-flops to allow data flow in transparent or clocked modes.

Data flow in each direction is controlled by output-enable ( $\overline{\text{OEAB}}$  and  $\overline{\text{OEBA}}$ ), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. When OEAB is high, the outputs are active. When OEAB is low, the outputs are in the high-impedance state.

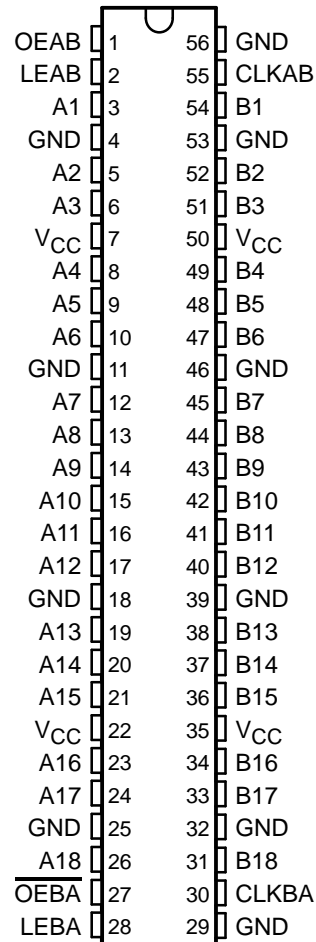
Data flow for B to A is similar to that of A to B but uses  $\overline{\text{OEBA}}$ , LEBA, and CLKBA. The output enables are complementary ( $\overline{\text{OEAB}}$  is active high and  $\overline{\text{OEBA}}$  is active low).

The B-port outputs, which are designed to source or sink up to 12 mA, include 25- $\Omega$  series resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The SN74ABT162501 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

SN54ABT162501 . . . WD PACKAGE  
SN74ABT162501 . . . DGG OR DL PACKAGE  
(TOP VIEW)



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# SN54ABT162501, SN74ABT162501

## 18-BIT UNIVERSAL BUS TRANSCEIVERS

### WITH 3-STATE OUTPUTS

SCBS243B – SEPTEMBER 1992 – REVISED JULY 1994

#### description (continued)

The SN54ABT162501 is characterized over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74ABT162501 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

FUNCTION TABLE<sup>†</sup>

INPUTS				OUTPUT
OEAB	LEAB	CLKAB	A	B
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↑	L	L
H	L	↑	H	H
H	L	H	X	B <sub>0</sub> <sup>‡</sup>
H	L	L	X	B <sub>0</sub> <sup>§</sup>

<sup>†</sup> A-to-B data flow is shown: B-to-A flow is similar but uses OEBA, LEBA, and CLKBA.

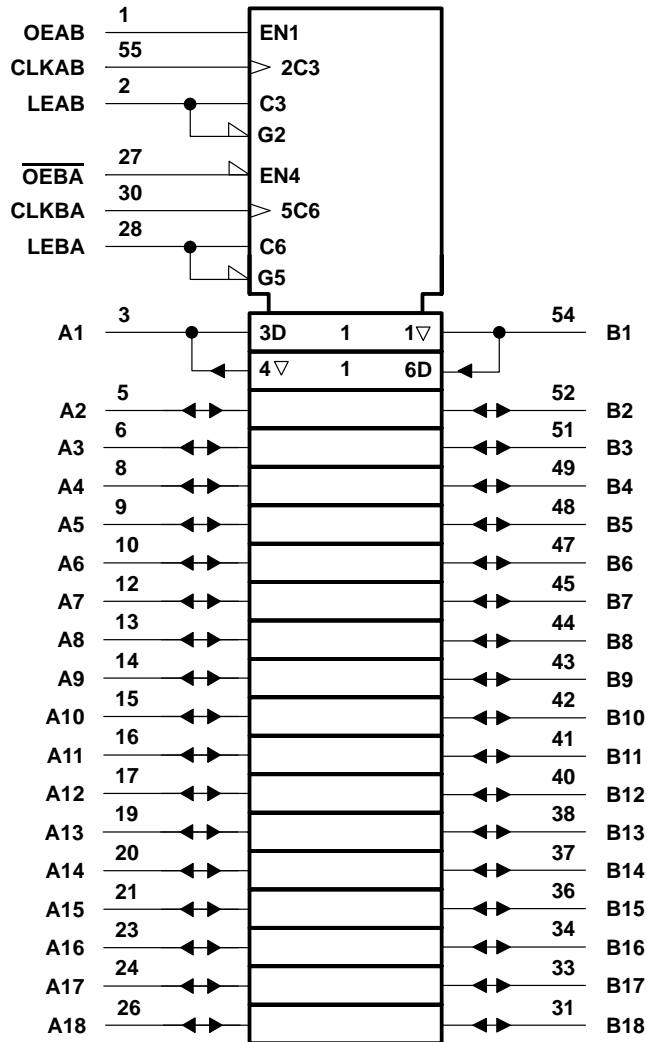
<sup>‡</sup> Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low.

<sup>§</sup> Output level before the indicated steady-state input conditions were established.

SN54ABT162501, SN74ABT162501  
18-BIT UNIVERSAL BUS TRANSCEIVERS  
WITH 3-STATE OUTPUTS

SCBS243B – SEPTEMBER 1992 – REVISED JULY 1994

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## SCBS243B – SEPTEMBER 1992 – REVISED JULY 1994

## 6-4

# SN54ABT162501, SN74ABT162501 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS243B – SEPTEMBER 1992 – REVISED JULY 1994

## recommended operating conditions (see Note 3)

			SN54ABT162501		SN74ABT162501		UNIT
			MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage		4.5	5.5	4.5	5.5	V
$V_{IH}$	High-level input voltage		2		2		V
$V_{IL}$	Low-level input voltage			0.8		0.8	V
$V_I$	Input voltage		0	$V_{CC}$	0	$V_{CC}$	V
$I_{OH}$	High-level output current	A port		–24		–32	mA
		B port		–12		–12	
$I_{OL}$	Low-level output current	A port		48		64	mA
		B port		12		12	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		200		200		$\mu s/V$
$T_A$	Operating free-air temperature		–55	125	–40	85	$^{\circ}C$

NOTE 3: Unused or floating pins (input or I/O) must be held high or low.

# SN54ABT162501, SN74ABT162501

## 18-BIT UNIVERSAL BUS TRANSCEIVERS

### WITH 3-STATE OUTPUTS

SCBS243B – SEPTEMBER 1992 – REVISED JULY 1994

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	T <sub>A</sub> = 25°C			SN54ABT162501		SN74ABT162501		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V <sub>IK</sub>		V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA			-1.2		-1.2		-1.2	V
V <sub>OH</sub>	A port	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -3 mA	2.5			2.5		2.5		V
		V <sub>CC</sub> = 5 V, I <sub>OH</sub> = -3 mA	3			3		3		
		V <sub>CC</sub> = 4.5 V	I <sub>OH</sub> = -24 mA	2		2				
			I <sub>OH</sub> = -32 mA	2*				2		
	B port	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -1 mA	3.35			3.3		3.35		
		V <sub>CC</sub> = 5 V, I <sub>OH</sub> = -1 mA	3.85			3.8		3.85		
		V <sub>CC</sub> = 4.5 V	I <sub>OH</sub> = -3 mA	3.1		3		3.1		
			I <sub>OH</sub> = -12 mA	2.6				2.6		
V <sub>OL</sub>	A port	V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 48 mA		0.55	0.55				V
			I <sub>OL</sub> = 64 mA		0.55*				0.55	
	B port	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 12 mA			0.8	0.8		0.8		
I <sub>I</sub>	Control inputs	V <sub>CC</sub> = 0 to 5.5 V, V <sub>I</sub> = V <sub>CC</sub> or GND			±1	±1		±1		μA
	A or B ports	V <sub>CC</sub> = 2.1 V to 5.5 V, V <sub>I</sub> = V <sub>CC</sub> or GND			±20	±20		±20		
I <sub>OZPU</sub>		V <sub>CC</sub> = 0 to 2.1 V, V <sub>O</sub> = 0.5 V to 2.7 V, $\overline{\text{OE}}$ or OE = X			±50	±50		±50		μA
I <sub>OZPD</sub>		V <sub>CC</sub> = 2.1 V to 0, V <sub>O</sub> = 0.5 V to 2.7 V, $\overline{\text{OE}}$ or OE = X			±50	±50		±50		μA
I <sub>OZH</sub> ‡		V <sub>CC</sub> = 2.1 V to 5.5 V, V <sub>O</sub> = 2.7 V, $\overline{\text{OE}}$ ≥ 2 V or OE ≤ 0.8 V§			10	10		10		μA
I <sub>OZL</sub> ‡		V <sub>CC</sub> = 2.1 V to 5.5 V, V <sub>O</sub> = 0.5 V, $\overline{\text{OE}}$ ≥ 2 V or OE ≤ 0.8 V§			-10	-10		-10		μA
I <sub>off</sub>		V <sub>CC</sub> = 0, V <sub>I</sub> or V <sub>O</sub> ≤ 4.5 V			±100			±100		μA
I <sub>CEX</sub>	Outputs high	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 5.5 V			50	50		50		μA
I <sub>O</sub> ¶	A port	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.5 V	-50	-110	-180	-50	-180	-50	-180	mA
	B port	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.5 V	-25	-55	-90	-25	-90	-25	-90	
I <sub>CC</sub>	A or B ports	V <sub>CC</sub> = 5.5 V, I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND	Outputs high		3	3		3		mA
			Outputs low		36	36		36		
			Outputs disabled		3	3		3		
ΔI <sub>CC</sub> #		V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND			50	50		50		μA
C <sub>i</sub>	Control inputs	V <sub>I</sub> = 2.5 V or 0.5 V			3					pF
C <sub>io</sub>	A or B ports	V <sub>O</sub> = 2.5 V or 0.5 V			9					pF

\* On products compliant to MIL-STD-883, Class B, this parameter does not apply.

† All typical values are at V<sub>CC</sub> = 5 V.

‡ The parameters I<sub>OZH</sub> and I<sub>OZL</sub> include the input leakage current.

§ For V<sub>CC</sub> between 2.1 V and 4 V, OE should be less than or equal to 0.5 V to ensure a low state.

¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

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# SN54ABT162501, SN74ABT162501

## 18-BIT UNIVERSAL BUS TRANSCEIVERS

### WITH 3-STATE OUTPUTS

SCBS243B – SEPTEMBER 1992 – REVISED JULY 1994

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

				SN54ABT162501		SN74ABT162501		UNIT
				MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency			0	150	0	150	MHz
t <sub>w</sub>	Pulse duration	LEAB or LEBA high		3		3		ns
		CLKAB or CLKBA high or low		3.3		3.3		
t <sub>su</sub>	Setup time	A before CLKAB↑		4.3		4.3		ns
		B before CLKBA↑		4.3		4.3		
		A before LEAB↓ or B before LEBA↓	CLK high	2.5		2.5		
			CLK low	1		1		
t <sub>h</sub>	Hold time	A after CLKAB↑ or B after CLKBA↑		0		0		ns
		A after LEAB↓ or B after LEBA↓		2		2		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$			SN54ABT162501		SN74ABT162501		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{\text{max}}$			150	200		150		150		MHz
$t_{\text{PLH}}$	A or B	B or A	1.5	2.6	4	1.5	5.1	1.5	4.8	ns
$t_{\text{PHL}}$			2	3.4	5.2	2	6.1	2	5.7	
$t_{\text{PLH}}$	LEAB or LEBA	B or A	2	3.3	4.8	2	6.1	2	5.6	ns
$t_{\text{PHL}}$			2	3.8	5.2	2	6.4	2	5.9	
$t_{\text{PLH}}$	CLKAB or CLKBA	B or A	1.5	3.5	4.7	1.5	6	1.5	5.5	ns
$t_{\text{PHL}}$			1.5	3.5	4.8	1.5	5.8	1.5	5.3	
$t_{\text{PZH}}$	OEAB or $\overline{\text{OEBA}}$	B or A	1.5	3.4	4.6	1.5	5.6	1.5	5.3	ns
$t_{\text{PZL}}$			2	3.8	4.7	2	5.6	2	5.4	
$t_{\text{PHZ}}$	OEAB or $\overline{\text{OEBA}}$	B or A	2	4.5	5.7	2	6.9	2	6.5	ns
$t_{\text{PLZ}}$			1.5	3.8	5.3	1.5	6.3	1.5	5.8	

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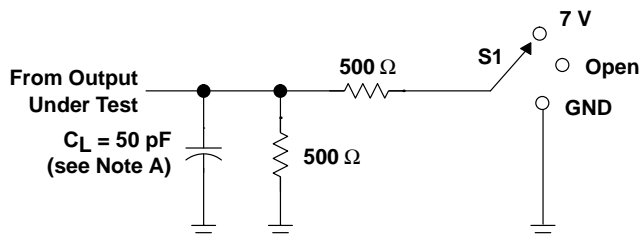
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## 18-BIT UNIVERSAL BUS TRANSCEIVERS

### WITH 3-STATE OUTPUTS

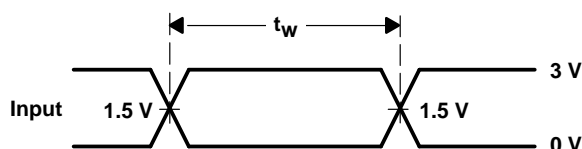
SCBS243B – SEPTEMBER 1992 – REVISED JULY 1994

#### PARAMETER MEASUREMENT INFORMATION

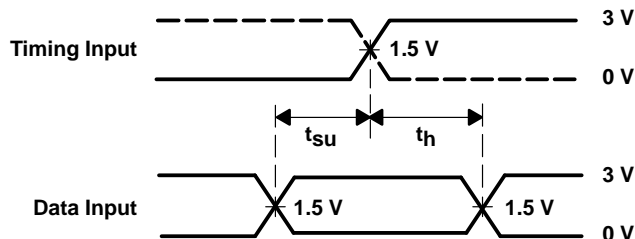


LOAD CIRCUIT FOR OUTPUTS

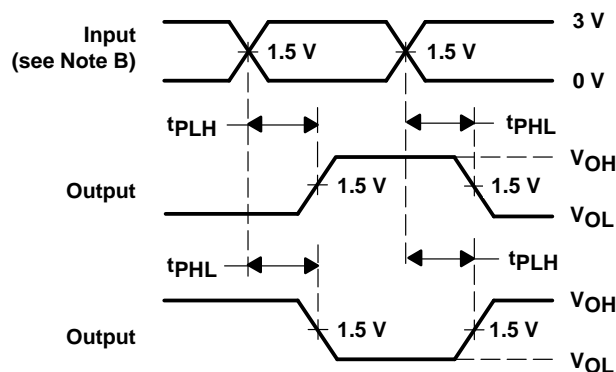
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	7 V
$t_{PHZ}/t_{PZH}$	Open



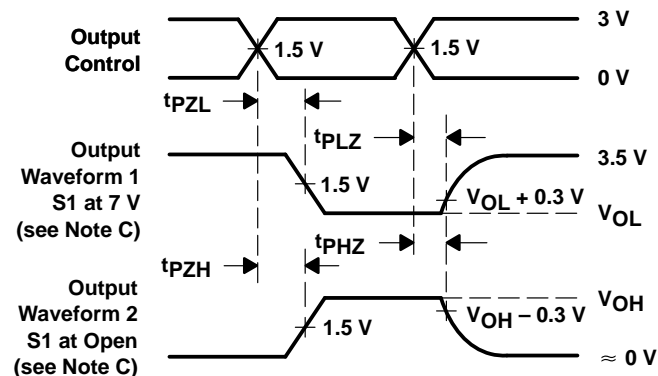
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



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