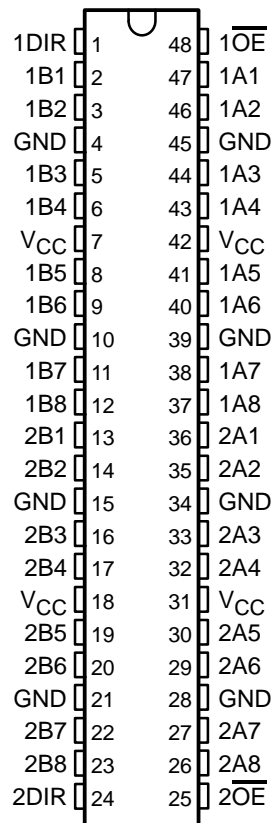


# SN54LVT162245, SN74LVT162245 3.3-V ABT 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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- A-Port Outputs Have Equivalent 22- $\Omega$  Series Resistors, So No External Resistors Are Required
- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Members of the Texas Instruments *Widebus*™ Family
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V  $V_{CC}$ )
- Support Unregulated Battery Operation Down to 2.7 V
- Typical  $V_{OLP}$  (Output Ground Bounce) < 0.8 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Support Live Insertion
- Distributed  $V_{CC}$  and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

SN54LVT162245 . . . WD PACKAGE  
SN74LVT162245 . . . DGG OR DL PACKAGE  
(TOP VIEW)



## description

The 'LVT162245 are 16-bit (dual-octal) noninverting 3-state transceivers designed for low-voltage (3.3-V)  $V_{CC}$  operation, but with the capability to provide a TTL interface to a 5-V system environment.

These devices can be used as two 8-bit transceivers or one 16-bit transceiver. The devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ( $\overline{OE}$ ) input can be used to disable the device so that the buses are effectively isolated.

The A-port outputs, which are designed to source or sink up to 8 mA, include 22- $\Omega$  series resistors to reduce overshoot and undershoot.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.



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# SN54LVT162245, SN74LVT162245

## 3.3-V ABT 16-BIT BUS TRANSCEIVERS

### WITH 3-STATE OUTPUTS

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#### description (continued)

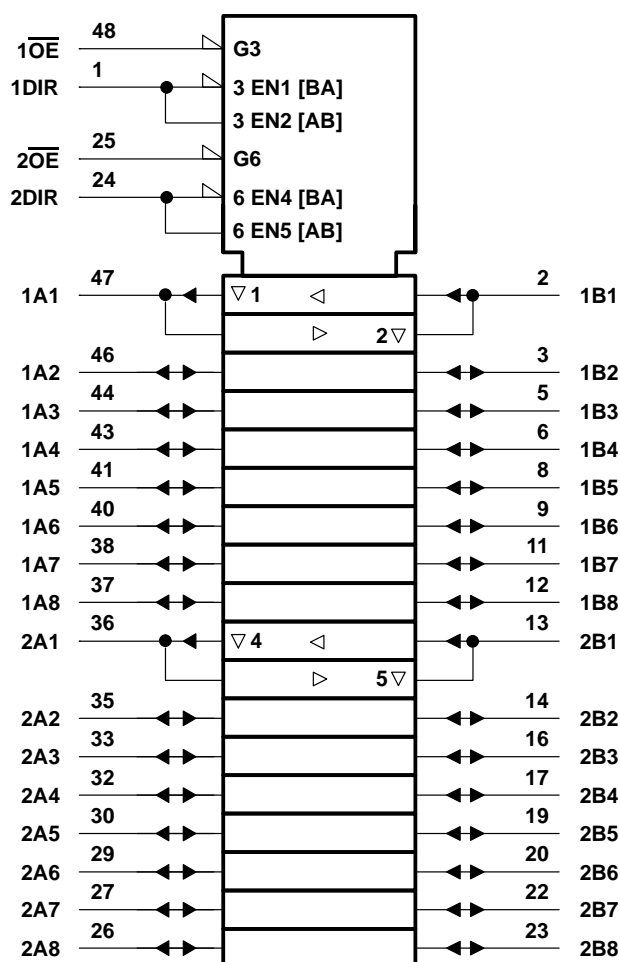
The SN74LVT162245 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the input/output (I/O) pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVT162245 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74LVT162245 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

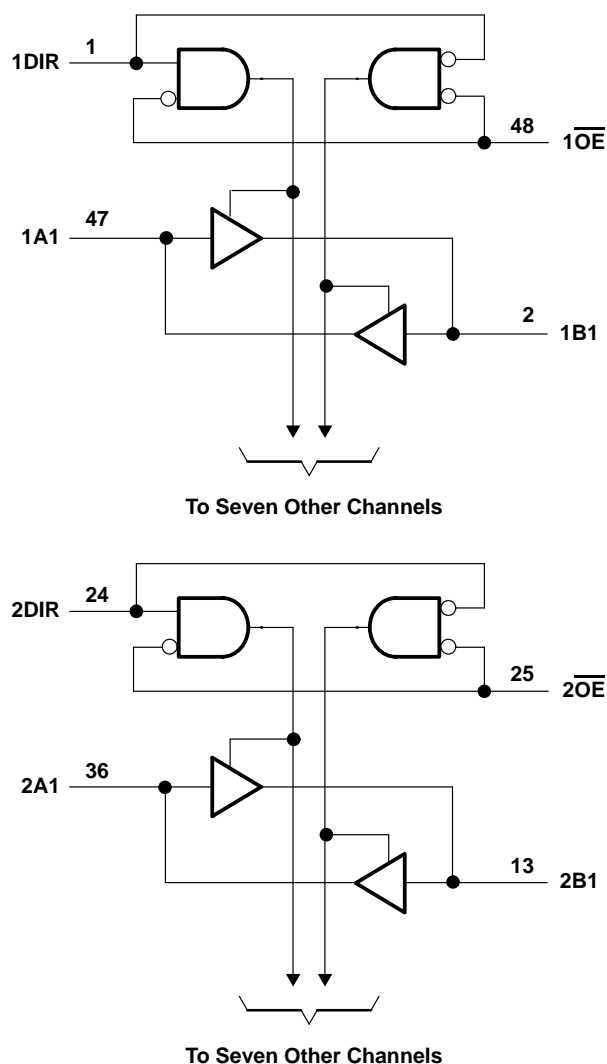
**FUNCTION TABLE**  
(each 8-bit section)

INPUTS		OPERATION
$\overline{\text{OE}}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

#### logic symbol†



#### logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

# SN54LVT162245, SN74LVT162245

## 3.3-V ABT 16-BIT BUS TRANSCEIVERS

### WITH 3-STATE OUTPUTS

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#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	–0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, $V_O$ (see Note 1)	–0.5 V to 7 V
Current into any output in the low state, $I_O$ : SN54LVT162245 (B port)	96 mA
SN74LVT162245 (B port)	128 mA
A port	30 mA
Current into any output in the high state, $I_O$ (see Note 2): SN54LVT162245 (B port)	48 mA
SN74LVT162245 (B port)	64 mA
A port	30 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ )	–50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 3): DGG package	0.85 W
DL package	1.2 W
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
  2. This current flows only when the output is in the high state and  $V_O > V_{CC}$ .
  3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

#### recommended operating conditions (see Note 4)

			SN54LVT162245		SN74LVT162245		UNIT
			MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage		2.7	3.6	2.7	3.6	V
V <sub>IH</sub>	High-level input voltage		2		2		V
V <sub>IL</sub>	Low-level input voltage			0.8		0.8	V
V <sub>I</sub>	Input voltage			5.5		5.5	V
I <sub>OH</sub>	High-level output current	B port	−24		−32		mA
		A port	−8		−8		
I <sub>OL</sub>	Low-level output current	A port	8		8		mA
		B port	48		64		
Δt/Δv	Input transition rise or fall rate	Outputs enabled	10		10		ns/V
T <sub>A</sub>	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

# SN54LVT162245, SN74LVT162245

## 3.3-V ABT 16-BIT BUS TRANSCEIVERS

### WITH 3-STATE OUTPUTS

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS		SN54LVT162245			SN74LVT162245			UNIT		
				MIN	TYP†	MAX	MIN	TYP†	MAX			
V <sub>IK</sub>		V <sub>CC</sub> = 2.7 V, I <sub>I</sub> = −18 mA		−1.2			−1.2			V		
V <sub>OH</sub>	A port	V <sub>CC</sub> = 3 V, I <sub>OH</sub> = −8 mA		2			2			V		
	B port	V <sub>CC</sub> = MIN to MAX‡, I <sub>OH</sub> = −100 μA		V <sub>CC</sub> − 0.2			V <sub>CC</sub> − 0.2					
		V <sub>CC</sub> = 2.7 V, I <sub>OH</sub> = −8 mA		2.4			2.4					
		V <sub>CC</sub> = 3 V	I <sub>OH</sub> = −24 mA		2							
			I <sub>OH</sub> = −32 mA					2				
V <sub>OL</sub>	A port	V <sub>CC</sub> = 3 V, I <sub>OL</sub> = 8 mA		0.8			0.8			V		
	B port	V <sub>CC</sub> = 2.7 V	I <sub>OL</sub> = 100 μA		0.2			0.2				
			I <sub>OL</sub> = 24 mA		0.5			0.5				
		V <sub>CC</sub> = 3 V	I <sub>OL</sub> = 16 mA		0.4			0.4				
			I <sub>OL</sub> = 32 mA		0.5			0.5				
			I <sub>OL</sub> = 48 mA		0.55							
			I <sub>OL</sub> = 64 mA					0.55				
	I <sub>I</sub>	Control pins	V <sub>CC</sub> = 3.6 V, V <sub>I</sub> = V <sub>CC</sub> or GND		±1			±1			μA	
V <sub>CC</sub> = 0 or MAX‡, V <sub>I</sub> = 5.5 V			10			10						
A or B ports		V <sub>CC</sub> = 3.6 V	V <sub>I</sub> = 5.5 V		20			20				
			V <sub>I</sub> = V <sub>CC</sub>		5			5				
			V <sub>I</sub> = 0		−10			−10				
I <sub>off</sub>		V <sub>CC</sub> = 0, V <sub>I</sub> or V <sub>O</sub> = 0 to 4.5 V					±100			μA		
I <sub>I</sub> (hold)	A or B ports	V <sub>CC</sub> = 3 V	V <sub>I</sub> = 0.8 V		75			75			μA	
			V <sub>I</sub> = 2 V		−75			−75				
		V <sub>CC</sub> = 3.6 V, V <sub>I</sub> = 0 to 3.6 V		±500			±500					
I <sub>OZH</sub>		V <sub>CC</sub> = 3.6 V, V <sub>O</sub> = 3 V		1			1			μA		
I <sub>OZL</sub>		V <sub>CC</sub> = 3.6 V, V <sub>O</sub> = 0.5 V		−1			−1			μA		
I <sub>CC</sub>		V <sub>CC</sub> = 3.6 V, V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0,		Outputs high		0.09			0.09			mA
				Outputs low		5			5			
				Outputs disabled		0.09			0.09			
ΔI <sub>CC</sub> §		V <sub>CC</sub> = 3 V to 3.6 V, One input at V <sub>CC</sub> − 0.6 V, Other inputs at V <sub>CC</sub> or GND		0.2			0.2			mA		
C <sub>i</sub>		V <sub>I</sub> = 3 V or 0		4			4			pF		
C <sub>io</sub>		V <sub>O</sub> = 3 V or 0		10.5			10.5			pF		

† All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND.

**SN54LVT162245, SN74LVT162245**  
**3.3-V ABT 16-BIT BUS TRANSCEIVERS**  
**WITH 3-STATE OUTPUTS**

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**switching characteristics over recommended operating free-air temperature range,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT162245				SN74LVT162245				UNIT	
			V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V			V <sub>CC</sub> = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN		MAX
t <sub>PLH</sub>	A	B	1	4.3	5.2		1	2.4	4.1	5		ns
t <sub>PHL</sub>			1	4.3	5.3		1	2.3	4.1	5.2		
t <sub>PLH</sub>	B	A	2	5.7	7.1		2	3.5	5.5	6.9		ns
t <sub>PHL</sub>			1.9	4.8	5.7		1.9	3.3	4.7	5.6		
t <sub>PZH</sub>	$\overline{OE}$	B	1	5.5	6.9		1	3	5.3	6.8		ns
t <sub>PZL</sub>			1	5.4	6.8		1	3.1	5.2	6.7		
t <sub>PZH</sub>	$\overline{OE}$	A	2.3	7.5	9.6		2.3	4.5	7.2	9.4		ns
t <sub>PZL</sub>			2.4	6.9	8.4		2.4	4.1	6.6	8.2		
t <sub>PHZ</sub>	$\overline{OE}$	B	2.7	6.7	7.4		2.7	4.6	6.4	7.2		ns
t <sub>PLZ</sub>			2.6	6	6.3		2.6	4.3	5.8	6.1		
t <sub>PHZ</sub>	$\overline{OE}$	A	3.3	7.6	8.3		3.3	5	7.3	8		ns
t <sub>PLZ</sub>			3.4	6.9	7.5		3.4	5	6.7	7.1		

† All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

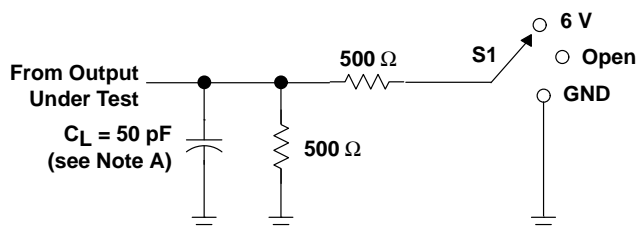
# SN54LVT162245, SN74LVT162245

## 3.3-V ABT 16-BIT BUS TRANSCEIVERS

### WITH 3-STATE OUTPUTS

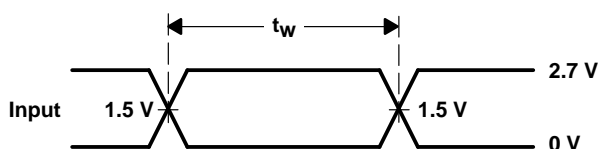
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#### PARAMETER MEASUREMENT INFORMATION

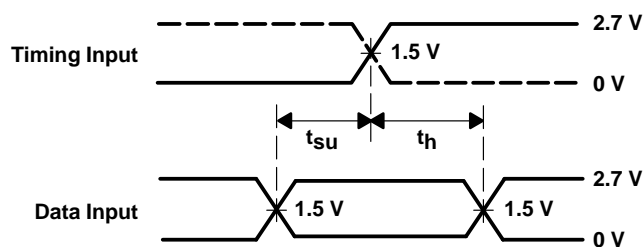


LOAD CIRCUIT FOR OUTPUTS

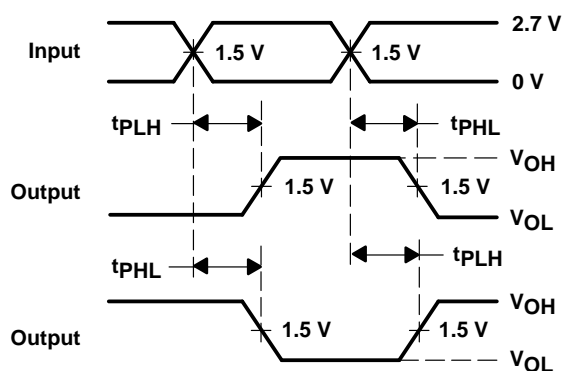
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND



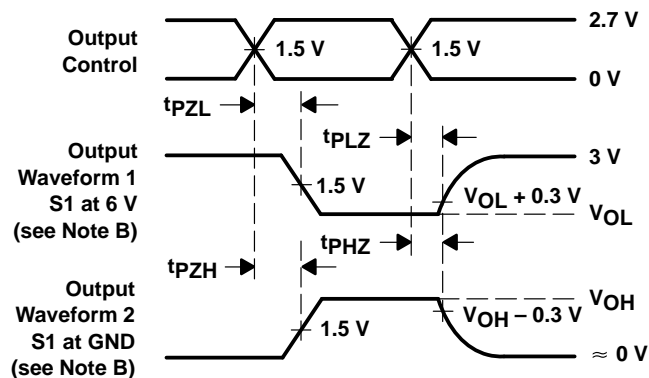
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns.  
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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