

SN74LVT16835

3.3-V ABT 18-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS

SCBS309C – MARCH 1994 – REVISED JULY 1995

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Member of the Texas Instruments *Widebus™* Family
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Supports Live Insertion
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages Using 25-mil Center-to-Center Spacings

description

The SN74LVT16835 is an 18-bit universal bus driver designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

Data flow from A to Y is controlled by the output-enable (\overline{OE}) input. This device operates in the transparent mode when the latch-enable (LE) input is high. The A data is latched if the clock (CLK) input is held at a high or low logic level. If LE is low, the A-bus data is stored in the latch/flip-flop on the low-to-high transition of the clock. When \overline{OE} is high, the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVT16835 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the input/output (I/O) pins and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74LVT16835 is characterized for operation from -40°C to 85°C .

DGG OR DL PACKAGE (TOP VIEW)

NC	1	56	GND
NC	2	55	NC
Y1	3	54	A1
GND	4	53	GND
Y2	5	52	A2
Y3	6	51	A3
V_{CC}	7	50	V_{CC}
Y4	8	49	A4
Y5	9	48	A5
Y6	10	47	A6
GND	11	46	GND
Y7	12	45	A7
Y8	13	44	A8
Y9	14	43	A9
Y10	15	42	A10
Y11	16	41	A11
Y12	17	40	A12
GND	18	39	GND
Y13	19	38	A13
Y14	20	37	A14
Y15	21	36	A15
V_{CC}	22	35	V_{CC}
Y16	23	34	A16
Y17	24	33	A17
GND	25	32	GND
Y18	26	31	A18
\overline{OE}	27	30	CLK
LE	28	29	GND

NC – No internal connection



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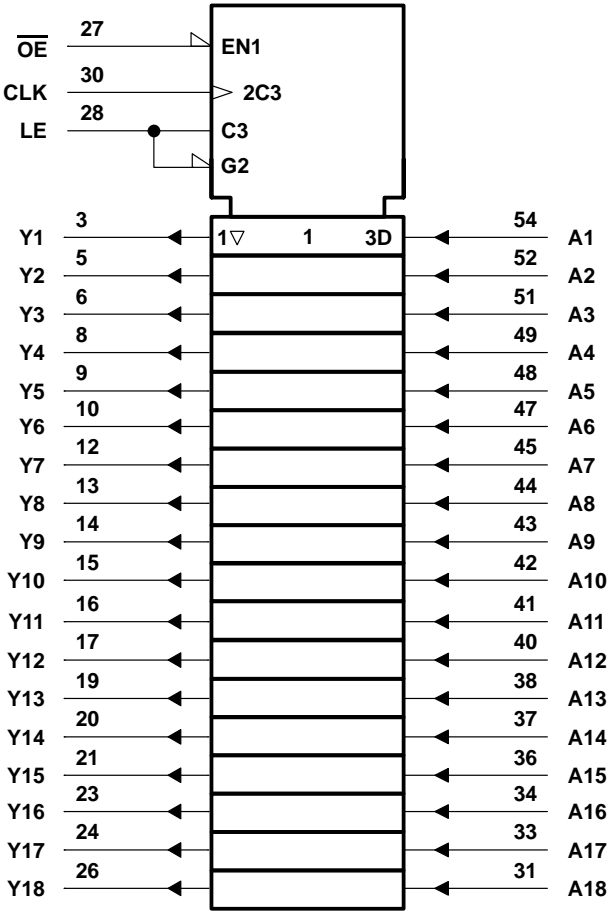
FUNCTION TABLE

INPUTS				OUTPUT Y
\overline{OE}	LE	CLK	A	
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	\uparrow	L	L
L	L	\uparrow	H	H
L	L	H	X	Y_0^\dagger
L	L	L	X	Y_0^\ddagger

† Output level before the indicated steady-state input conditions were established, provided that CLK was high before LE went low

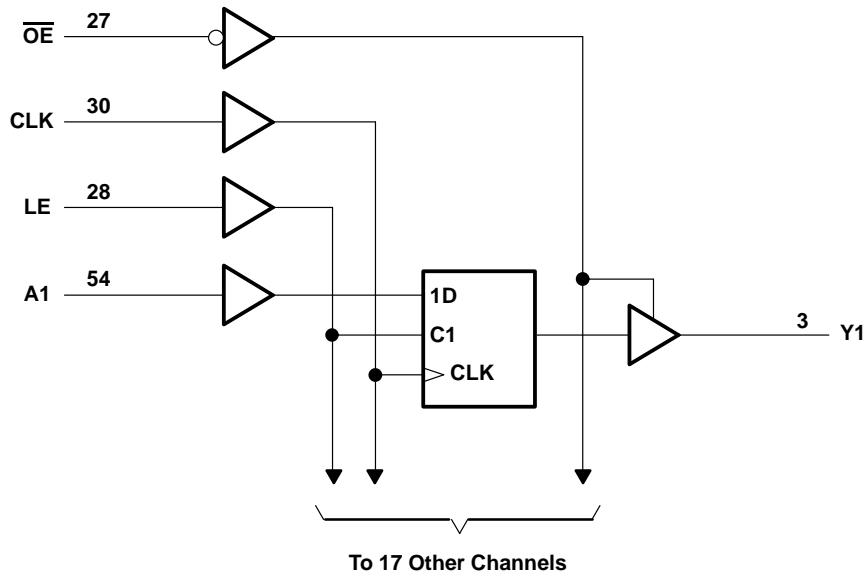
‡ Output level before the indicated steady-state input conditions were established

logic symbols



§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Current into any output in the low state, I_O	128 mA
Current into any output in the high state, I_{OH} (see Note 2)	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 3): DGG package	1 W
DL package	1.4 W
Operating free-air temperature range, T_A	–40°C to 85°C
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

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recommended operating conditions (see Note 4)

	MIN	MAX	UNIT
V _{CC} Supply voltage	2.7	3.6	V
V _{IH} High-level input voltage	2		V
V _{IL} Low-level input voltage		0.8	V
V _I Input voltage		5.5	V
I _{OH} High-level output current		–32	mA
I _{OL} Low-level output current		64	mA
Δt/Δv Input transition rise or fall rate	Outputs enabled		10 ns/V
T _A Operating free-air temperature	–40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V _{IK}	V _{CC} = 2.7 V, I _I = –18 mA			–1.2	V
V _{OH}	V _{CC} = MIN to MAX‡, I _{OH} = –100 μA	V _{CC} – 0.2			V
	V _{CC} = 2.7 V, I _{OH} = –8 mA	2.4			
	V _{CC} = 3 V, I _{OH} = –32 mA	2			
V _{OL}	V _{CC} = 2.7 V	I _{OL} = 100 μA		0.2	V
		I _{OL} = 24 mA		0.5	
	V _{CC} = 3 V	I _{OL} = 16 mA		0.4	
		I _{OL} = 32 mA		0.5	
		I _{OL} = 64 mA		0.55	
I _I	Control inputs	V _{CC} = 0 or MAX‡, V _I = 5.5 V		10	μA
		V _{CC} = 3.6 V, V _I = V _{CC} or GND		±1	
	A inputs	V _{CC} = 3.6 V, V _I = V _{CC}		1	
		V _I = 5.5 V		20	
I _{off}	V _{CC} = 0, V _I or V _O = 0 to 4.5 V			±100	μA
I _{I(hold)}	A inputs	V _{CC} = 3 V, V _I = 0.8 V		75	μA
		V _I = 2 V		–75	
I _{OZH}	V _{CC} = 3.6 V, V _O = 3 V			1	μA
I _{OZL}	V _{CC} = 3.6 V, V _O = 0.5 V			–1	μA
I _{CC}	V _{CC} = 3.6 V, V _I = V _{CC} or GND, I _O = 0,	Outputs high		0.12	mA
		Outputs low		5	
		Outputs disabled		0.12	
ΔI _{CC} §	V _{CC} = 3 V to 3.6 V, One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND			0.2	mA
C _i	Control inputs	V _I = 3 V or 0		3.5	pF
	Data pins			4.5	
C _O	V _O = 3 V or 0			11	pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.



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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency		0	150	0	125	MHz
t _w	Pulse duration	LE high	3.3		3.3		ns
		CLK high or low	3.3		3.3		
t _{su}	Setup time	Data before CLK↑	1.6		2.1		ns
		Data before LE↓, CLK high	2.6		1.9		
		Data before LE↓, CLK low	2		1.3		
t _h	Hold time	Data after CLK↑	2		2.1		ns
		Data after LE↓	0.9		1.2		

switching characteristics over recommended operating free-air temperature range, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$			$V_{CC} = 2.7\text{ V}$		UNIT
			MIN	TYP \dagger	MAX	MIN	MAX	
f_{max}			150			150		MHz
t_{PLH}	A	Y	1.7	3	5.4	6.8		ns
t_{PHL}			1.6	3.2	5.9	7.7		
t_{PLH}	LE	Y	2.3	4	7	8.5		ns
t_{PHL}			2.7	4.3	7.9	9.7		
t_{PLH}	CLK	Y	2.5	4.1	7.9	9.2		ns
t_{PHL}			3.5	5.4	8.9	10.4		
t_{PZH}	$\overline{\text{OE}}$	Y	1.2	3	5	5.9		ns
t_{PZL}			1.5	3	5.8	6.9		
t_{PHZ}	$\overline{\text{OE}}$	Y	2.7	4.6	7.4	8.3		ns
t_{PLZ}			2.8	4.7	6.7	7.2		

\dagger All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

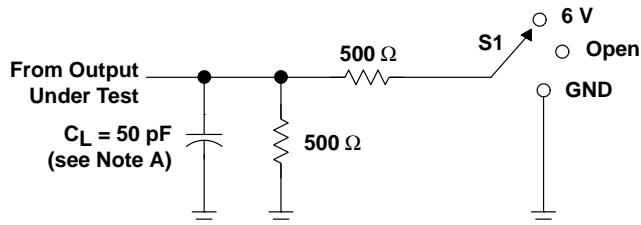
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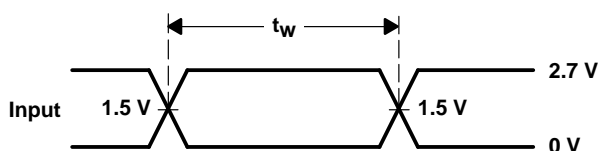
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PARAMETER MEASUREMENT INFORMATION

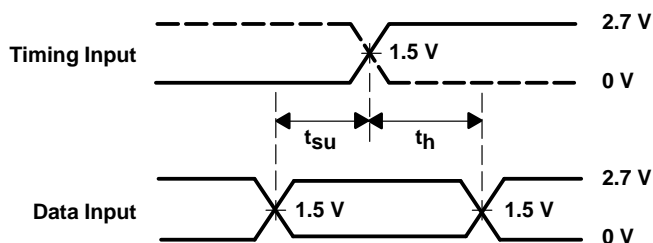


LOAD CIRCUIT FOR OUTPUTS

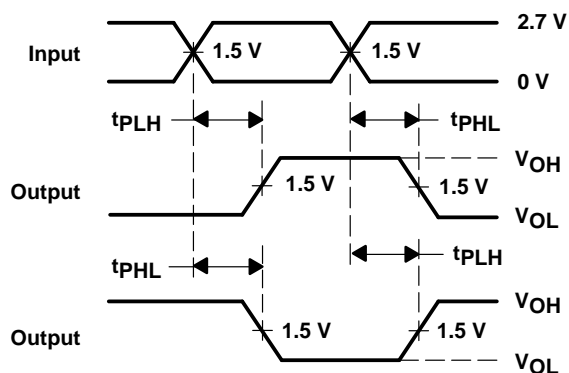
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



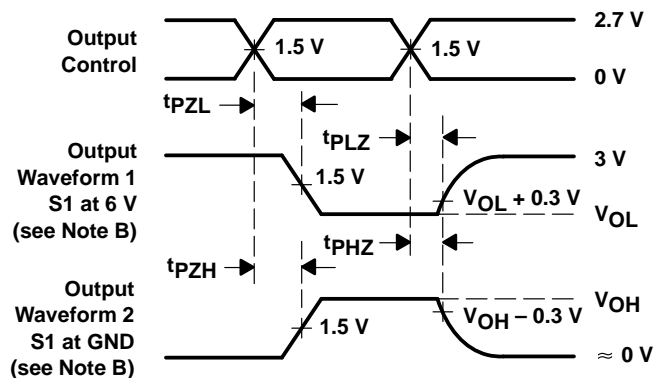
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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