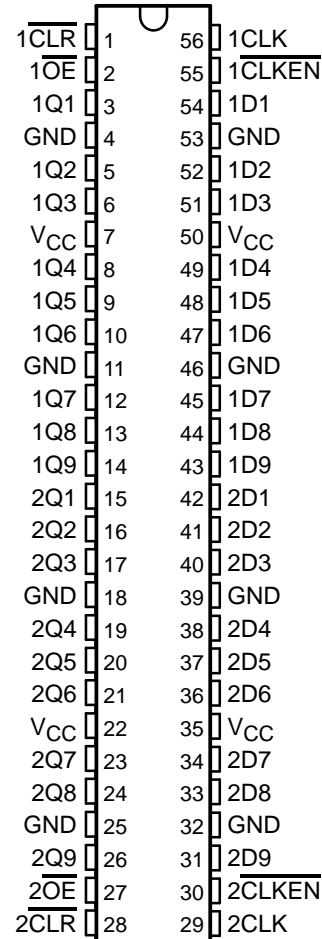


SN54ABT162823, SN74ABT162823 18-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

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- Output Ports Have Equivalent 25- Ω Series Resistors So No External Resistors Are Required
- Members of the Texas Instruments *Widebus*™ Family
- State-of-the-Art *EPIC-II B*™ BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Typical V_{OLP} (Output Ground Bounce) < 1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) Package and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

SN54ABT162823 . . . WD PACKAGE
SN74ABT162823 . . . DL PACKAGE
(TOP VIEW)



description

These 18-bit bus-interface flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

The 'ABT162823 can be used as two 9-bit flip-flops or one 18-bit flip-flop. With the clock-enable ($\overline{\text{CLKEN}}$) input low, the D-type flip-flops enter data on the low-to-high transitions of the clock. Taking $\overline{\text{CLKEN}}$ high disables the clock buffer, thus latching the outputs. Taking the clear ($\overline{\text{CLR}}$) input low causes the Q outputs to go low independently of the clock.

A buffered output-enable ($\overline{\text{OE}}$) input places the nine outputs in either a normal logic state (high or low level) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components. $\overline{\text{OE}}$ does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The outputs, which are designed to source or sink up to 12 mA, include 25- Ω series resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

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SN54ABT162823, SN74ABT162823

18-BIT BUS-INTERFACE FLIP-FLOPS

WITH 3-STATE OUTPUTS

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description (continued)

The SN74ABT162823 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT162823 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ABT162823 is characterized for operation from -40°C to 85°C .

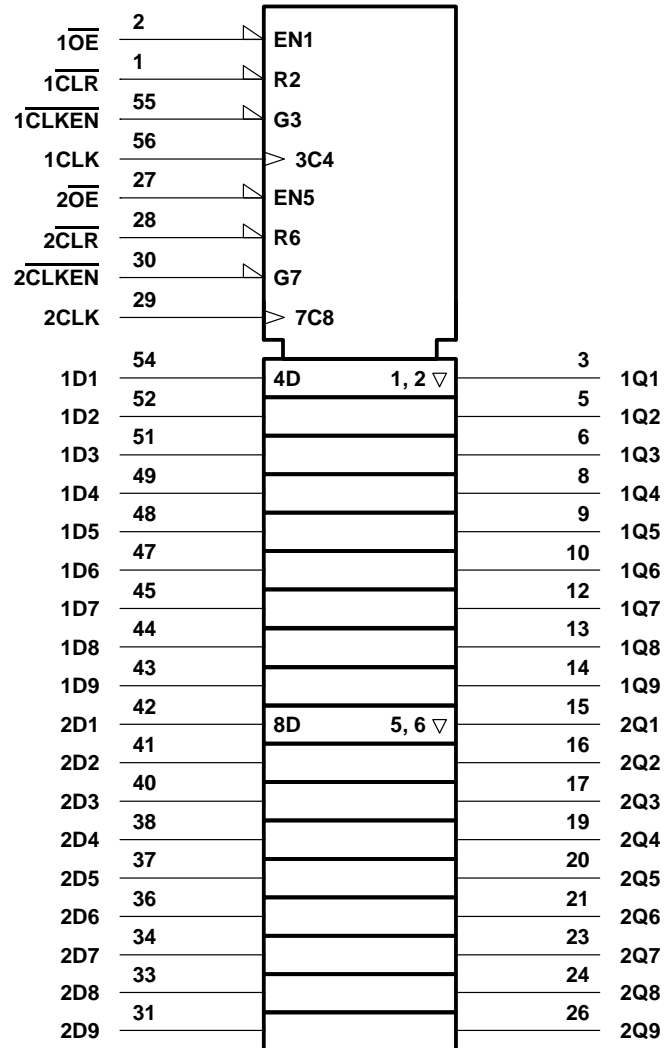
FUNCTION TABLE
(each 9-bit flip-flop)

INPUTS					OUTPUT
$\overline{\text{OE}}$	$\overline{\text{CLR}}$	$\overline{\text{CLKEN}}$	CLK	D	Q
L	L	X	X	X	L
L	H	L	\uparrow	H	H
L	H	L	\uparrow	L	L
L	H	L	L	X	Q_0
L	H	H	X	X	Q_0
H	X	X	X	X	Z

SN54ABT162823, SN74ABT162823
18-BIT BUS-INTERFACE FLIP-FLOPS
WITH 3-STATE OUTPUTS

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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

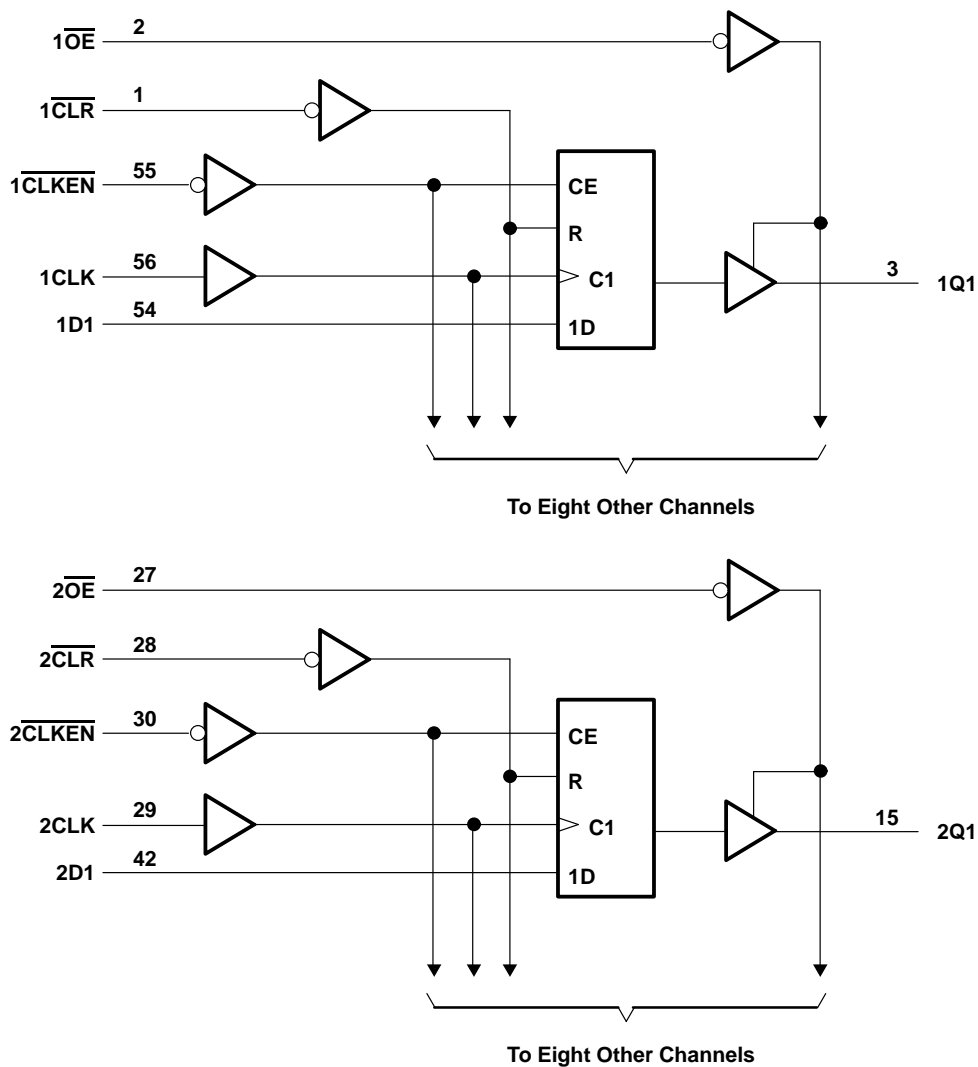
SN54ABT162823, SN74ABT162823

18-BIT BUS-INTERFACE FLIP-FLOPS

WITH 3-STATE OUTPUTS

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logic diagram (positive logic)



SN54ABT162823, SN74ABT162823

18-BIT BUS-INTERFACE FLIP-FLOPS

WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O	–0.5 V to 5.5 V
Current into any output in the low state, I_O	30 mA
Input clamp current, I_{IK} ($V_I < 0$)	–18 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2): DL package	1.4 W
Storage temperature range	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 3)

		SN54ABT162823		SN74ABT162823		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–12		–12	mA
I_{OL}	Low-level output current		12		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused or floating inputs must be held high or low.

SN54ABT162823, SN74ABT162823

18-BIT BUS-INTERFACE FLIP-FLOPS

WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T _A = 25°C			SN54ABT162823		SN74ABT162823		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA		-1.2			-1.2		-1.2		V
V _{OH}	V _{CC} = 4.5 V, I _{OH} = -1 mA		3.35			3.35		3.35		V
	V _{CC} = 5 V, I _{OH} = -1 mA		3.85			3.85		3.85		
	V _{CC} = 4.5 V	I _{OH} = -3 mA	3.1			3.1		3.1		
		I _{OH} = -12 mA	2.6*					2.6		
V _{OL}	V _{CC} = 4.5 V	I _{OL} = 8 mA	0.4		0.8	0.8		0.65		V
		I _{OL} = 12 mA						0.8		
I _I	V _{CC} = 5.5 V, V _I = V _{CC} or GND		±1			±1		±1		μA
I _{OZH}	V _{CC} = 5.5 V, V _O = 2.7 V		10			10		10		μA
I _{OZL}	V _{CC} = 5.5 V, V _O = 0.5 V		-10			-10		-10		μA
I _{off}	V _{CC} = 0, V _I or V _O ≤ 4.5 V		±100					±100		μA
I _{CEX}	V _{CC} = 5.5 V, V _O = 5.5 V	Outputs high	50			50		50		μA
I _O ‡	V _{CC} = 5.5 V, V _O = 2.5 V		-25	-55	-100	-25	-100	-25	-100	mA
I _{CC}	V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND	Outputs high	2			2		2		mA
		Outputs low	80			80		80		
		Outputs disabled	2			2		2		
ΔI _{CC} §	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND		1.5			1.5		1.5		mA
C _i	V _I = 2.5 V or 0.5 V		3							pF
C _O	V _O = 2.5 V or 0.5 V		8							pF

* On products compliant to MIL-STD-883, Class B, this parameter does not apply.

† All typical values are at V_{CC} = 5 V.

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

§ This is the increase in supply current for each input that is at the specified TTL-voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			V _{CC} = 5 V, T _A = 25°C		SN54ABT162823		SN74ABT162823		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency		0	150	0	150	0	150	MHz
t _w	Pulse duration	CLR low	3.3		3.3		3.3		ns
		CLK high or low	3.3		3.3		3.3		
t _{su}	Setup time before CLK↑	CLR inactive	1.6		2		1.6		ns
		Data	1.7		1.7		1.7		
		CLKEN low	2.8		2.8		2.8		
t _h	Hold time after CLK↑	Data	1.2		1.2		1.2		ns
		CLKEN low	0.6		0.6		0.6		

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SN54ABT162823, SN74ABT162823 18-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$			SN54ABT162823		SN74ABT162823		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{\max}			150			150		150		MHz
t_{PLH}	CLK	Q	2.3	4.6	6.2	2.3	8.4	2.3	7.5	ns
t_{PHL}			2.8	4.6	6.1	2.8	7.1	2.8	6.7	
t_{PHL}	$\overline{\text{CLR}}$	Q	2.8	5	6.2	2.8	7.2	2.8	7	ns
t_{PZH}	$\overline{\text{OE}}$	Q	1.7	3.8	4.9	1.7	5.8	1.7	5.6	ns
t_{PZL}			3	5	6.1	3	7.2	3	7	
t_{PHZ}	$\overline{\text{OE}}$	Q	2.7	4.8	6.1	2.7	7.3	2.7	6.6	ns
t_{PLZ}			1.9	4.6	6.7	1.9	10.2	1.9	9	

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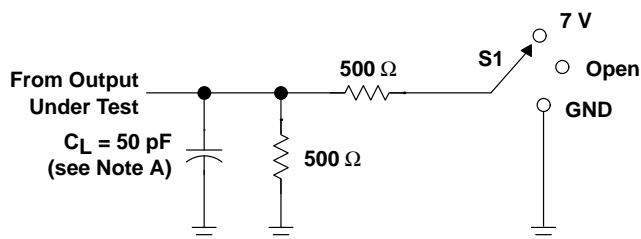
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18-BIT BUS-INTERFACE FLIP-FLOPS

WITH 3-STATE OUTPUTS

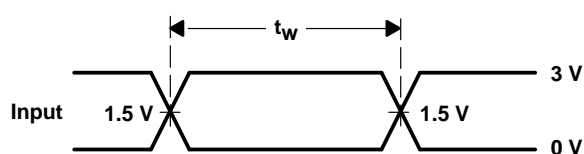
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PARAMETER MEASUREMENT INFORMATION

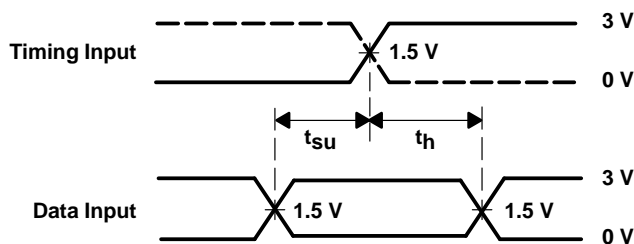


LOAD CIRCUIT FOR OUTPUTS

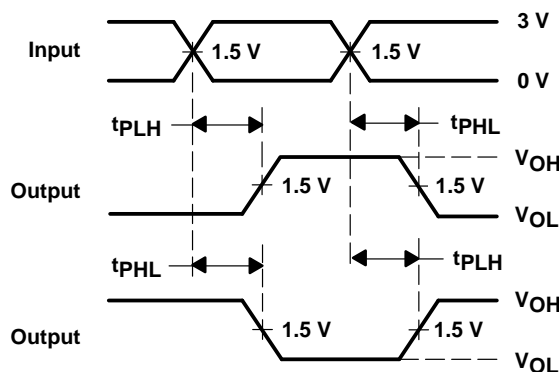
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



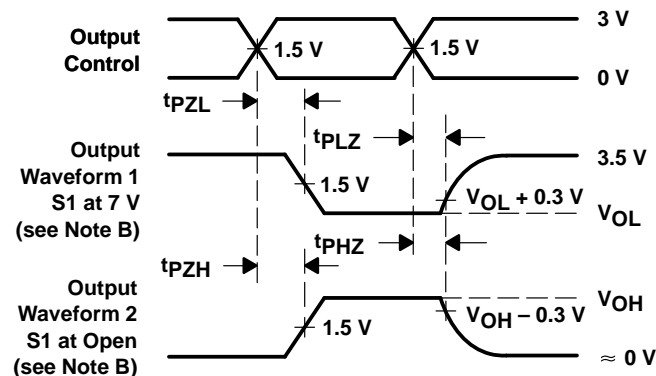
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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