

# SN54ABT5402A, SN74ABT5402A 11-BIT LINE/MEMORY DRIVERS WITH 3-STATE OUTPUTS

SCBS660 – FEBRUARY 1996

- Output Ports Have 25-Ω Series Resistors, So No External Resistors Are Required
- State-of-the-Art *EPIC-II B*™ BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical  $V_{OLP}$  (Output Ground Bounce) < 1 V at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OLV}$  (Output Undershoot) < 0.5 V at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$
- Package Options Include Plastic Small-Outline (DW) Packages and Ceramic Chip Carriers (FK) and DIPs (JT)

## description

These 12-bit buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

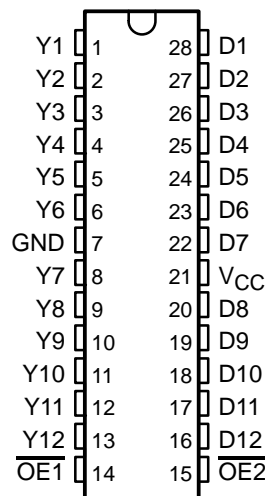
The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable ( $\overline{OE1}$  or  $\overline{OE2}$ ) input is high, all 12 outputs are in the high-impedance state.

The outputs, which are designed to source or sink up to 12 mA, include 25-Ω series resistors to reduce overshoot and undershoot.

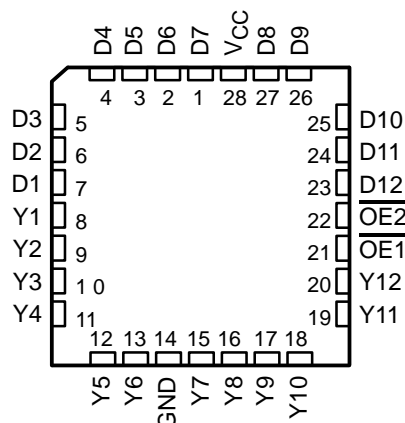
To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT5402A is characterized for operation over the full military temperature range of  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ . The SN74ABT5402A is characterized for operation from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .

SN54ABT5402A . . . JT PACKAGE  
SN74ABT5402A . . . DW PACKAGE  
(TOP VIEW)



SN54ABT5402A . . . FK PACKAGE  
(TOP VIEW)



FUNCTION TABLE

INPUTS			OUTPUT Y
$\overline{OE1}$	$\overline{OE2}$	D	
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z



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**TEXAS  
INSTRUMENTS**

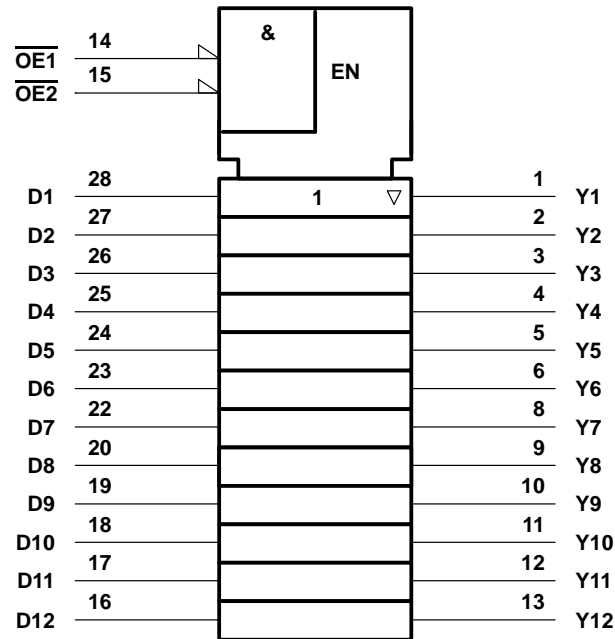
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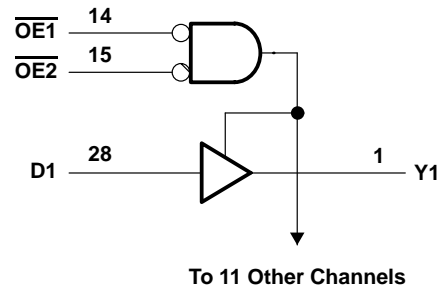
SN54ABT5402A, SN74ABT5402A  
11-BIT LINE/MEMORY DRIVERS  
WITH 3-STATE OUTPUTS

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logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984  
and IEC Publication 617-12.

Pin numbers shown are for the DW and JT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, $V_O$	-0.5 V to 5.5 V
Current into any output in the low state, $I_O$	30 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	-18 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ )	-50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2): DW package	1.2 W
Storage temperature range, $T_{stg}$	-65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.  
For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 3)

			SN54ABT5402A		SN74ABT5402A		UNIT
			MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage		4.5	5.5	4.5	5.5	V
$V_{IH}$	High-level input voltage		2		2		V
$V_{IL}$	Low-level input voltage			0.8		0.8	V
$V_I$	Input voltage		0	$V_{CC}$	0	$V_{CC}$	V
$I_{OH}$	High-level output current			-12		-12	mA
$I_{OL}$	Low-level output current			12		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
$T_A$	Operating free-air temperature		-55	125	-40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T <sub>A</sub> = 25°C			SN54ABT5402A		SN74ABT5402A		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = −18 mA					−1.2		−1.2		−1.2	V
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = −1 mA			3.35	3.7		3.3		3.35		V
	V <sub>CC</sub> = 5 V, I <sub>OH</sub> = −1 mA			3.85	4.2		3.8		3.85		
	V <sub>CC</sub> = 4.5 V	I <sub>OH</sub> = −3 mA					3		3.1		
		I <sub>OH</sub> = −12 mA		2.6					2.6		
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 8 mA						0.8		0.65	V
		I <sub>OL</sub> = 12 mA							0.8		
I <sub>I</sub>	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = V <sub>CC</sub> or GND					±1		±1		±1	μA
I <sub>OZH</sub>	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.7 V					10		10		10	μA
I <sub>OZL</sub>	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0.5 V					−10		−10		−10	μA
I <sub>off</sub>	V <sub>CC</sub> = 0, V <sub>I</sub> or V <sub>O</sub> ≤ 4.5 V					±100				±100	μA
I <sub>CEX</sub>	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 5.5 V		Outputs high			50		50		50	μA
I <sub>O</sub>	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.5 V			−25	−45	−100	−25	−100	−25	−100	mA
I <sub>OS</sub> ‡	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0			−50		−200	−50	−200	−50	−200	mA
I <sub>CC</sub>	V <sub>CC</sub> = 5.5 V, I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND		Outputs high		5	50		50		50	μA
			Outputs low		39	48		48		48	mA
			Outputs disabled		1	50		50		50	μA
ΔI <sub>CC</sub> §	V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND	Data inputs	Outputs enabled			1.5		1.5		1.5	mA
			Outputs disabled			0.05		0.05		0.05	
		Control inputs			1.5		1.5		1.5		
C <sub>I</sub>	V <sub>I</sub> = 2.5 V or 0.5 V				3						pF
C <sub>O</sub>	V <sub>O</sub> = 2.5 V or 0.5 V				8						pF

† All typical values are at  $V_{CC} = 5\text{ V}$ .

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND.

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## 11-BIT LINE/MEMORY DRIVERS

### WITH 3-STATE OUTPUTS

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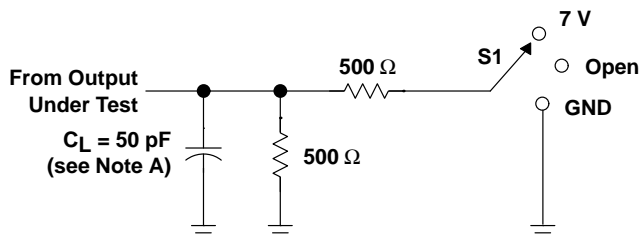
switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$			SN54ABT5402A		SN74ABT5402A		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	D	Y	2	4.5	5.2	2	6.3	2	6.2	ns
$t_{PHL}$			1.5	3.7	5	1.5	5.7	1.5	5.6	
$t_{PZH}$	$\overline{OE}$	Y	2.5	5.7	7.6	2.5	8.8	2.5	8.7	ns
$t_{PZL}$			2	4.4	6.3	2	7.6	2	7.5	
$t_{PHZ}$	$\overline{OE}$	Y	1.5	3.6	4.4	1.5	5.5	1.5	5.2	ns
$t_{PLZ}$			1.5	4.2	5.4	1.5	7.4	1.5	6.9	



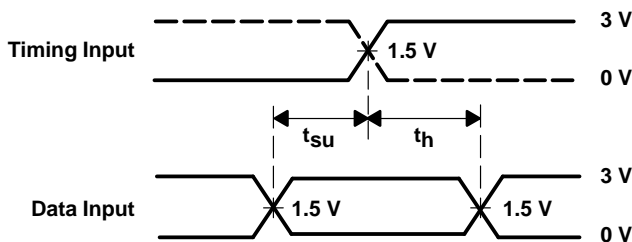
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## PARAMETER MEASUREMENT INFORMATION

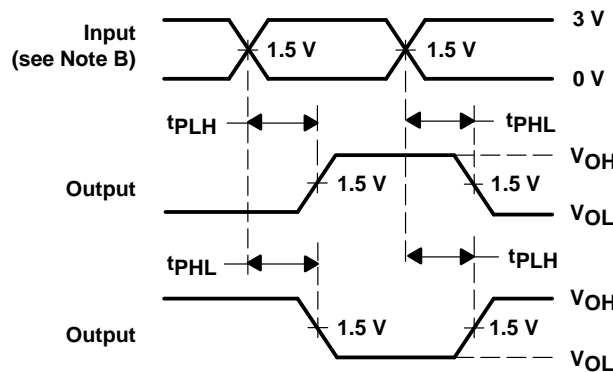


LOAD CIRCUIT

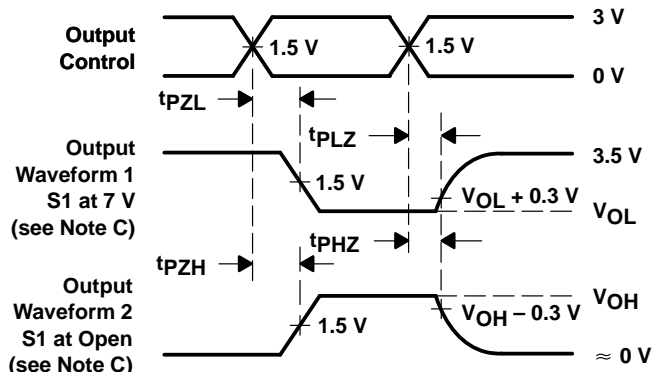
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	7 V
$t_{PHZ}/t_{PZH}$	Open



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.
- B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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