

SN74CBT3257

QUADRUPL 2-BIT TO 1-BIT FET MULTIPLEXER/DEMULTIPLEXER

SCDS017D – MAY 1995 – REVISED AUGUST 1996

- Functionally Equivalent to QS3257
- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Control Input Levels
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

description

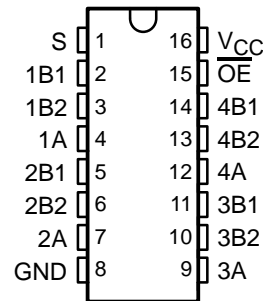
The SN74CBT3257 is a quadruple 2-bit to 1-bit high-speed TTL-compatible FET demultiplexer/multiplexer. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

\overline{OE} and S select the appropriate B1 and B2 outputs for the A-input data.

The SN74CBT3257 is available in TI's shrink small-outline (DB) and thin shrink small-outline (PW) packages, which provide the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74CBT3257 is characterized for operation from -40°C to 85°C .

D, DB, OR PW PACKAGE
(TOP VIEW)



FUNCTION TABLE

S	\overline{OE}	FUNCTION
X	H	Disconnect
L	L	A = B1
H	L	A = B2



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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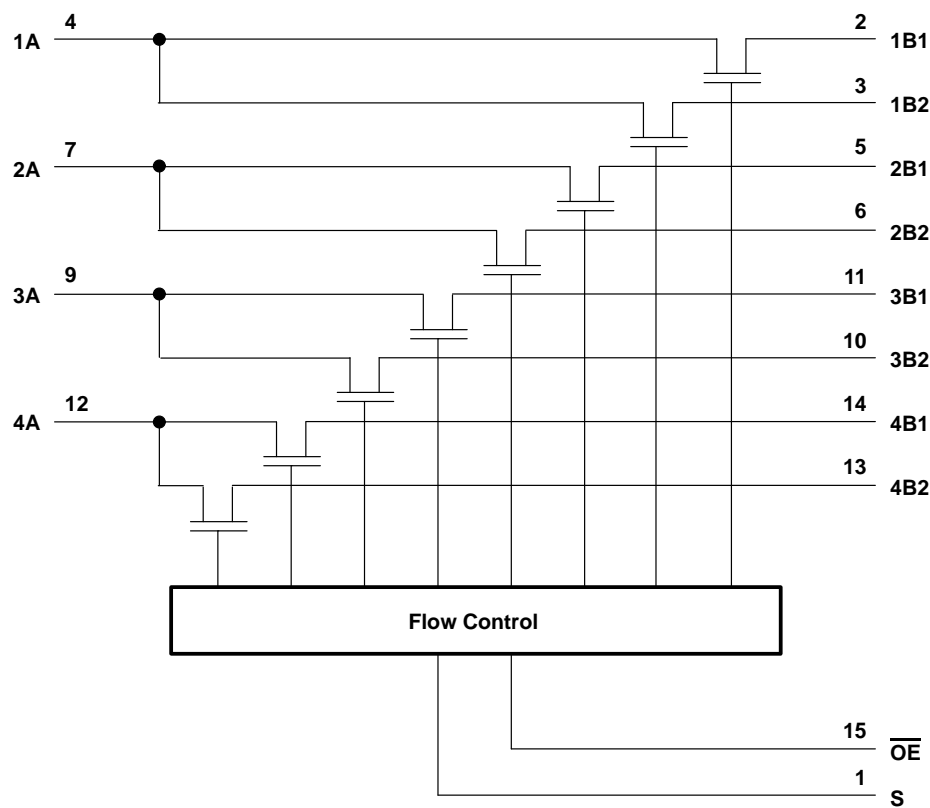
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logic diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Continuous channel current	128 mA
Input clamp current, I_K ($V_{I/O} < 0$)	–50 mA
Maximum power dissipation at $T_A = 55^{\circ}\text{C}$ (in still air) (see Note 2):	
D package	1.3 W
DB package	0.55 W
PW package	0.5 W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*.

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recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	-40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		$V_{CC} = 4.5\text{ V}$,	$I_I = -18\text{ mA}$			-1.2	V
I_I		$V_{CC} = 5.5\text{ V}$,	$V_I = 5.5\text{ V}$ or GND			± 1	μA
I_{CC}		$V_{CC} = 5.5\text{ V}$,	$I_O = 0$, $V_I = V_{CC}$ or GND			3	μA
ΔI_{CC}^\ddagger	Control pins	$V_{CC} = 5.5\text{ V}$,	One input at 3.4 V, Other inputs at V_{CC} or GND			2.5	mA
C_i	Control pins	$V_I = 3\text{ V}$ or 0				3.5	pF
$C_{io}(\text{OFF})$	A port	$V_O = 3\text{ V}$ or 0, $\overline{OE} = V_{CC}$				6.5	pF
	B port					4	
r_{on}^\S		$V_{CC} = 4\text{ V}$,	$V_I = 2.4\text{ V}$, $I_I = 15\text{ mA}$			14	Ω
		$V_{CC} = 4.5\text{ V}$	$V_I = 0$, $I_I = 64\text{ mA}$			5	
			$V_I = 0$, $I_I = 30\text{ mA}$			5	
			$V_I = 2.4\text{ V}$, $I_I = 15\text{ mA}$			10	

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

§ Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$		$V_{CC} = 4\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}^\parallel	A or B	B or A		0.25		0.25	ns
	S	A or B	1.6	5		5.5	
t_{en}	S	A or B	1.6	5.2		5.7	ns
t_{dis}	S	A or B	1	5		5.2	ns
t_{en}	\overline{OE}	A or B	1.8	5.1		5.6	ns
t_{dis}	\overline{OE}	A or B	2.2	5.5		5.5	ns

¶ This parameter is warranted but not production tested. The propagation delay is based on the RC time constant of the typical on-state resistance of the switch and a load capacitance of 50 pF, when driven by an ideal voltage source (zero output impedance).

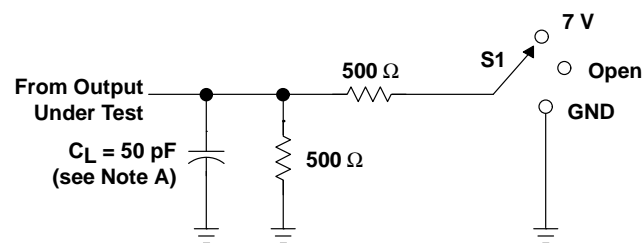


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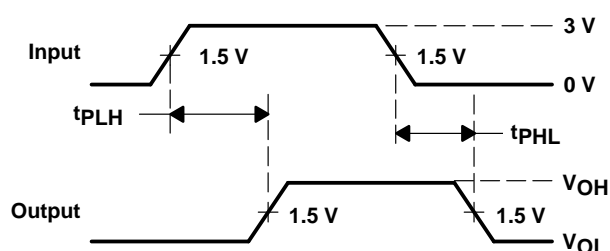
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PARAMETER MEASUREMENT INFORMATION

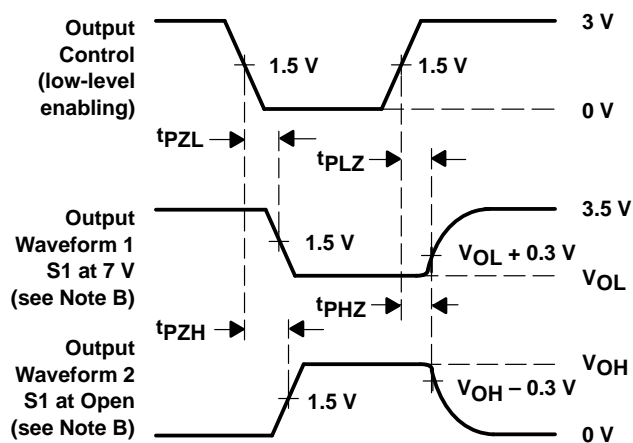


LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

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