

# SN74ALVCH16374 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

SCES021 – JULY 1995

- Member of the Texas Instruments *Widebus™* Family
- *EPIC™* (Enhanced-Performance Implanted CMOS) Submicron Process
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Bus Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

## description

This 16-bit edge-triggered D-type flip-flop is designed for 2.3-V to 3.6-V  $V_{CC}$  operation.

The SN74ALVCH16374 is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. It can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CLK) input, the Q outputs of the flip-flop take on the logic levels set up at the data (D) inputs.  $\overline{OE}$

can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.  $\overline{OE}$  does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

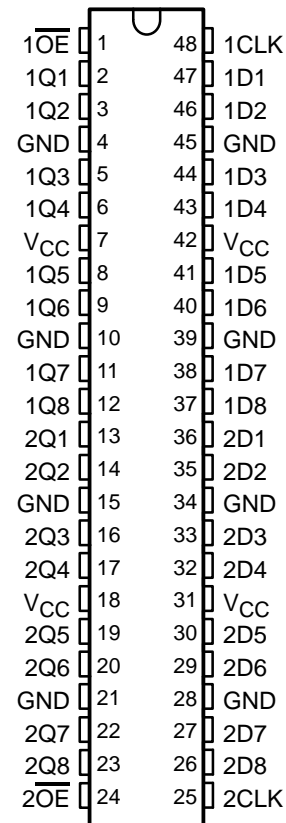
To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16374 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVCH16374 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

DGG OR DL PACKAGE  
(TOP VIEW)



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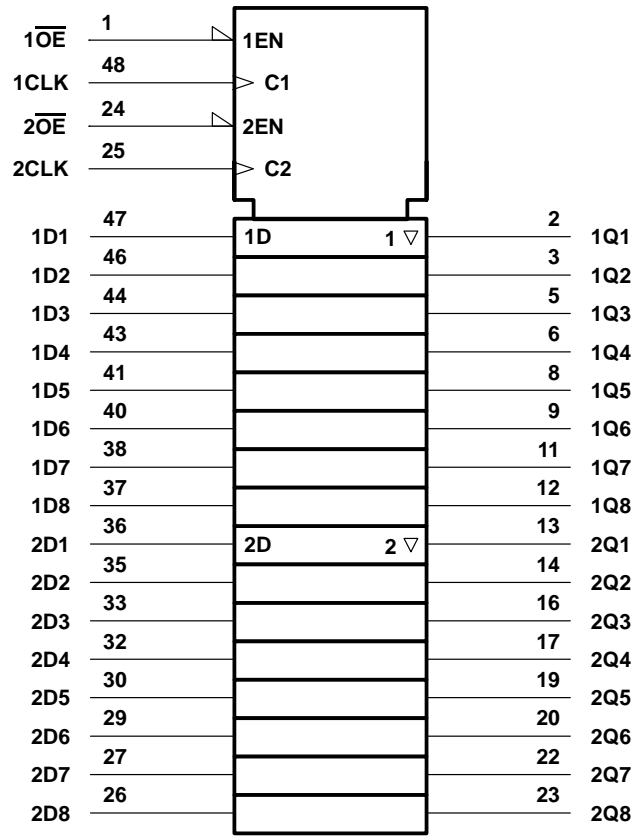
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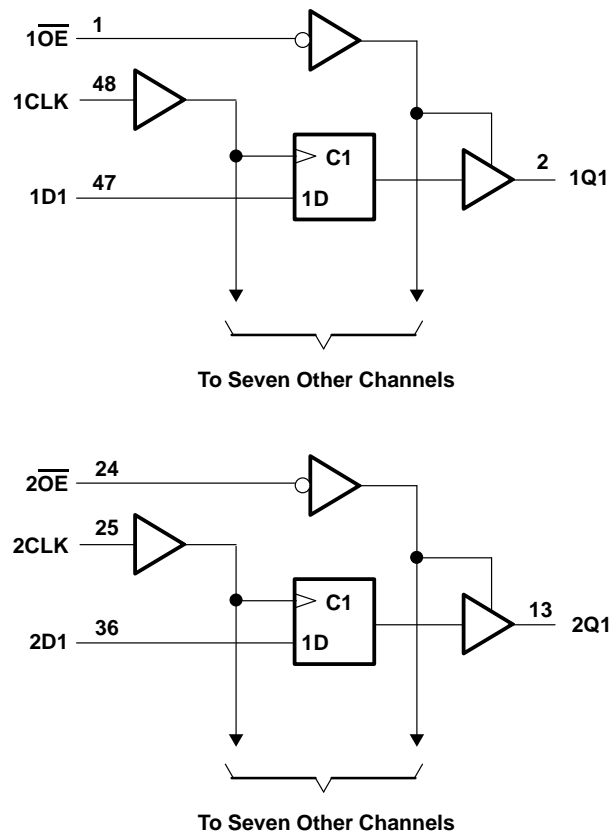
FUNCTION TABLE  
(each flip-flop)

INPUTS			OUTPUT Q
$\overline{OE}$	CLK	D	
L	$\uparrow$	H	H
L	$\uparrow$	L	L
L	H or L	X	$Q_0$
H	X	X	Z

## logic symbol†



## logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$	–0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 4.6 V
Output voltage range, $V_O$ (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±50 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±50 mA
Continuous current through each $V_{CC}$ or GND	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 3): DGG package	0.85 W
DL package	1.2 W
Storage temperature range, $T_{stg}$	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. This value is limited to 4.6 V maximum.  
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

**recommended operating conditions (see Note 4)**

			MIN	MAX	UNIT
$V_{CC}$	Supply voltage		2.3	3.6	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2.3$ V to 2.7 V	1.7		V
		$V_{CC} = 2.7$ V to 3.6 V	2		
$V_{IL}$	Low-level input voltage	$V_{CC} = 2.3$ V to 2.7 V		0.7	V
		$V_{CC} = 2.7$ V to 3.6 V		0.8	
$V_I$	Input voltage		0	$V_{CC}$	V
$V_O$	Output voltage		0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 2.3$ V		–12	mA
		$V_{CC} = 2.7$ V		–12	
		$V_{CC} = 3$ V		–24	
$I_{OL}$	Low-level output current	$V_{CC} = 2.3$ V		12	mA
		$V_{CC} = 2.7$ V		12	
		$V_{CC} = 3$ V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
$T_A$	Operating free-air temperature		–40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.



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## 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP

### WITH 3-STATE OUTPUTS

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub> <sup>†</sup>	MIN	TYP <sup>‡</sup>	MAX	UNIT
V <sub>OH</sub>	I <sub>OH</sub> = –100 µA	MIN to MAX	V <sub>CC</sub> – 0.2			V
	I <sub>OH</sub> = –6 mA, V <sub>IH</sub> = 1.7 V	2.3 V	2			
	I <sub>OH</sub> = –12 mA	V <sub>IH</sub> = 1.7 V	2.3 V		1.7	
		V <sub>IH</sub> = 2 V	2.7 V		2.2	
		V <sub>IH</sub> = 2 V	3 V		2.4	
	I <sub>OH</sub> = –24 mA, V <sub>IH</sub> = 2 V	3 V	2			
V <sub>OL</sub>	I <sub>OL</sub> = 100 µA	MIN to MAX			0.2	V
	I <sub>OL</sub> = 6 mA, V <sub>IL</sub> = 0.7 V	2.3 V			0.4	
	I <sub>OL</sub> = 12 mA, V <sub>IL</sub> = 0.7 V	2.3 V			0.7	
	I <sub>OL</sub> = 12 mA, V <sub>IL</sub> = 0.8 V	2.7 V			0.4	
	I <sub>OL</sub> = 24 mA, V <sub>IL</sub> = 0.8 V	3 V			0.55	
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.6 V			±5	µA
I <sub>I</sub> (hold)	V <sub>I</sub> = 0.7 V	2.3 V	45			µA
	V <sub>I</sub> = 1.7 V	2.3 V	–45			
	V <sub>I</sub> = 0.8 V	3 V	75			
	V <sub>I</sub> = 2 V	3 V	–75			
	V <sub>I</sub> = 0 to 3.6 V	3.6 V			±500	
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	3.6 V			±10	µA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	3.6 V			40	µA
ΔI <sub>CC</sub>	One input at V <sub>CC</sub> – 0.6 V, Other inputs at V <sub>CC</sub> or GND	3 V to 3.6 V			750	µA
C <sub>i</sub>	Control inputs	3.3 V	3			pF
	Data Inputs		6			
C <sub>O</sub>	Outputs	3.3 V	7			pF

<sup>†</sup> For conditions shown as MIN or MAX use the appropriate values under recommended operating conditions.

<sup>‡</sup> Typical values are measured at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

**timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 and 2)**

		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency	0	150	0	150	0	150	MHz
t <sub>w</sub>	Pulse duration, CLK high or low	3.3		3.3		3.3		ns
t <sub>su</sub>	Setup time, data before CLK↑	2.1		2.2		1.9		ns
t <sub>h</sub>	Hold time, data after CLK↑	0.6		0.5		0.5		ns



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**switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 and 2)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$f_{\text{max}}$			150		150		150		MHz
$t_{\text{pd}}$	CLK	Q	1	5.9	4.9		1	4.2	ns
$t_{\text{en}}$	CLK	Q	1	6.7	5.9		1	4.8	ns
$t_{\text{dis}}$	CLK	Q	1.7	5.5	4.7		1.2	4.3	ns

**operating characteristics,  $T_A = 25^\circ\text{C}$**

PARAMETER			TEST CONDITIONS	$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	UNIT
				TYP	TYP	
$C_{\text{pd}}$ Power dissipation capacitance	Outputs enabled	$C_L = 50\text{ pF}, \quad f = 10\text{ MHz}$		31	30	pF
	Outputs disabled			16	18	

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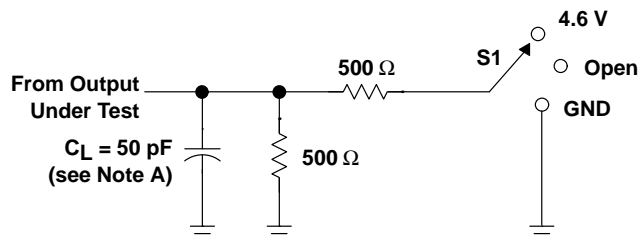
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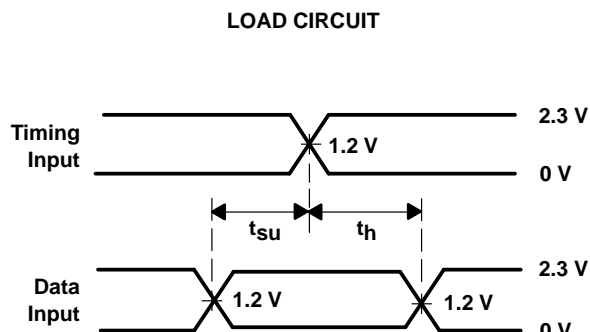
#### PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

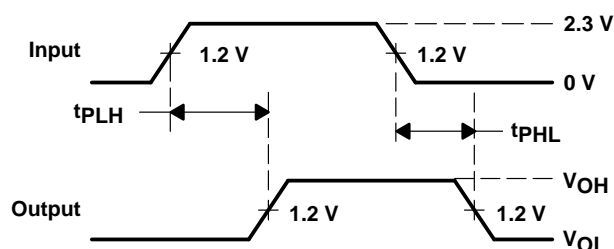


LOAD CIRCUIT

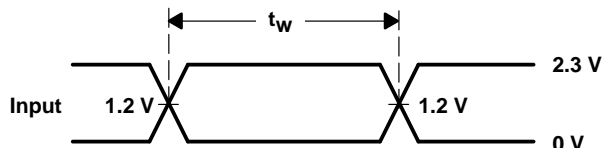
TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	4.6 V
$t_{PHZ}/t_{PZH}$	GND



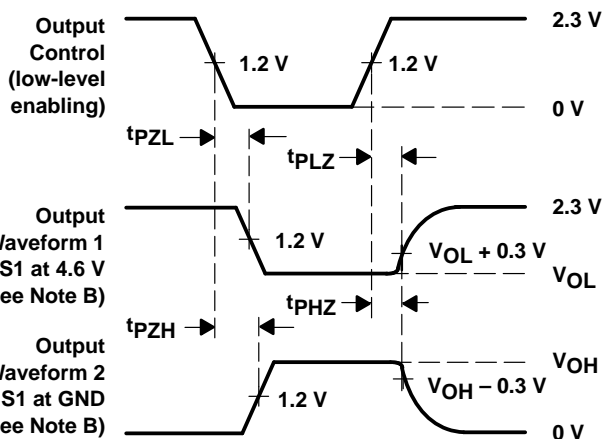
VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS  
PULSE DURATION



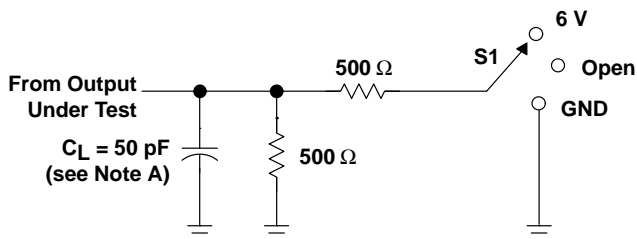
VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
  - The outputs are measured one at a time with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

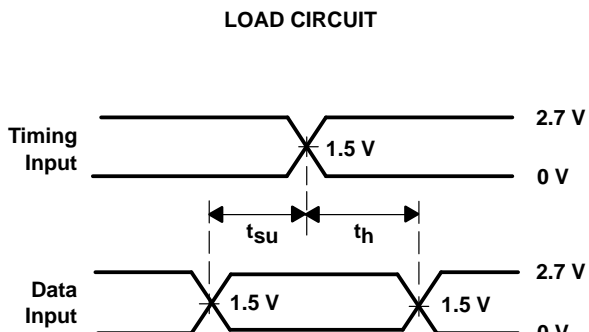
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7\text{ V}$  AND  $3.3\text{ V} \pm 0.3\text{ V}$

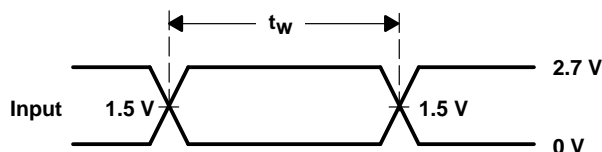


LOAD CIRCUIT

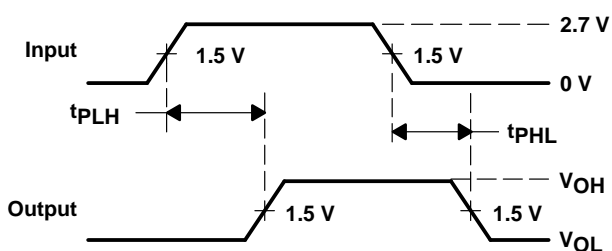
TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND



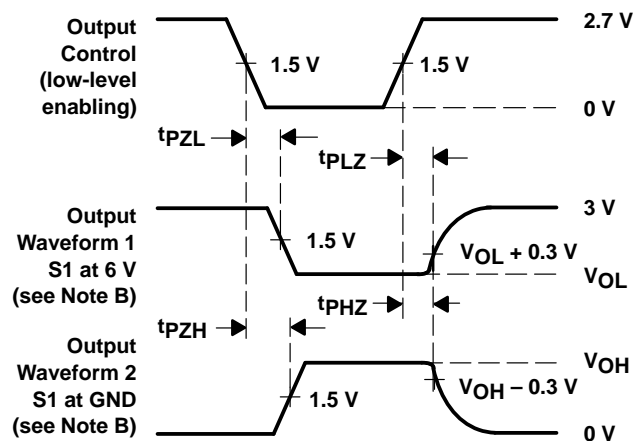
VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2.5\text{ ns}$ ,  $t_f \leq 2.5\text{ ns}$ .  
D. The outputs are measured one at a time with one transition per measurement.  
E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 2. Load Circuit and Voltage Waveforms

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