

SN74ALVCH16270

12-BIT TO 24-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS

SCES028 – JULY 1995

- Member of the Texas Instruments *Widebus™* Family
- *EPIC™* (Enhanced-Performance Implanted CMOS) Submicron Process
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 12-bit to 24-bit registered bus exchanger is designed for 2.3-V to 3.6-V V_{CC} operation.

The SN74ALVCH16270 is used in applications where data must be transferred from a narrow high-speed bus to a wide lower-frequency bus.

The device provides synchronous data exchange between the two ports. Data is stored in the internal registers on the low-to-high transition of the clock (CLK) input when the appropriate \overline{CLKEN} inputs are low. The select (SEL) line selects 1B or 2B data for the A outputs. For data transfer in the A-to-B direction, a two-stage pipeline is provided in the A-to-1B path, with a single storage register in the A to 2B path. Proper control of the \overline{CLKEN} inputs allows two sequential 12-bit words to be presented synchronously as a 24-bit word on the B port. Data flow is controlled by the active-low output enables (\overline{OE} , \overline{OEB}). The control terminals are registered to synchronize the bus direction changes with CLK.

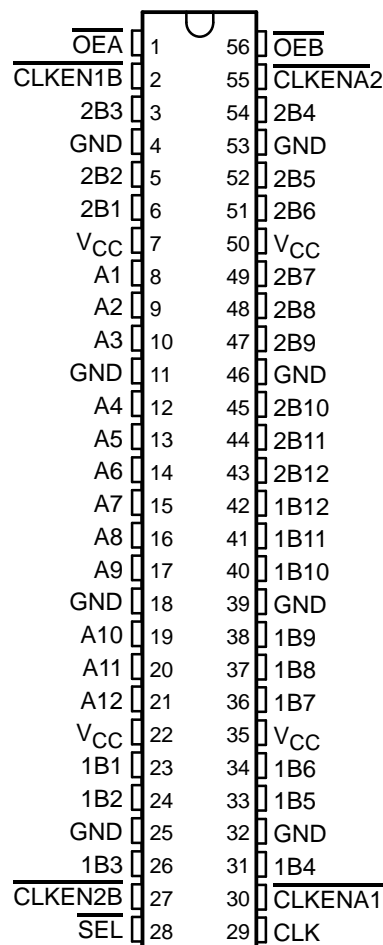
To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16270 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVCH16270 is characterized for operation from -40°C to 85°C .

DGG OR DL PACKAGE
(TOP VIEW)



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SCES028 – JULY 1995

Function Tables

OUTPUT ENABLE

INPUTS			OUTPUTS	
CLK	$\overline{\text{OEA}}$	$\overline{\text{OEB}}$	A	1B, 2B
↑	H	H	Z	Z
↑	H	L	Z	Active
↑	L	H	Active	Z
↑	L	L	Active	Active

A-TO-B STORAGE ($\overline{\text{OEB}} = \text{L}$)

INPUTS				OUTPUTS	
$\overline{\text{CLKENA1}}$	$\overline{\text{CLKENA2}}$	CLK	A	1B	2B
L	H	↑	L	L [†]	2B ₀ [‡]
L	H	↑	H	H [†]	2B ₀ [‡]
L	L	↑	L	L [†]	L
L	L	↑	H	H [†]	H
H	L	↑	L	1B ₀ [‡]	L
H	L	↑	H	1B ₀ [‡]	H
H	H	X	X	1B ₀ [‡]	2B ₀ [‡]

[†] Two CLK edges are needed to propagate data.

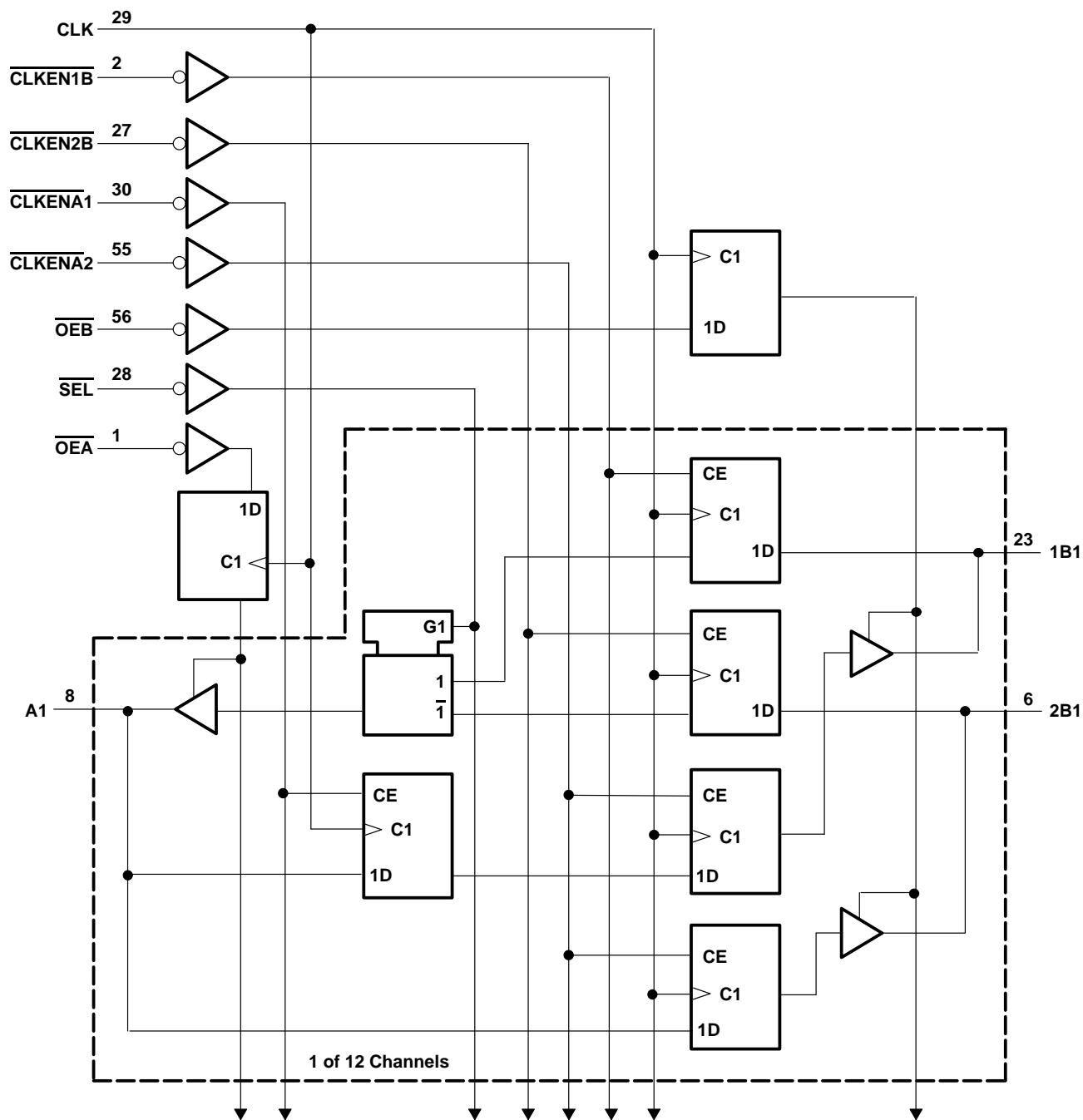
[‡] Output level before the indicated steady-state input conditions were established

B-TO-A STORAGE ($\overline{\text{OEA}} = \text{L}$)

INPUTS						OUTPUT A
$\overline{\text{CLKEN1B}}$	$\overline{\text{CLKEN2B}}$	CLK	$\overline{\text{SEL}}$	1B	2B	
H	X	X	H	X	X	A ₀ [‡]
X	H	X	L	X	X	A ₀ [‡]
L	X	↑	H	L	X	L
L	X	↑	H	H	X	H
X	L	↑	L	X	L	L
X	L	↑	L	X	H	H

[‡] Output level before the indicated steady-state input conditions were established

logic diagram (positive logic)



SN74ALVCH16270

12-BIT TO 24-BIT REGISTERED BUS EXCHANGER

WITH 3-STATE OUTPUTS

SCES028 – JULY 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I : Except I/O ports (see Note 1)	–0.5 V to 4.6 V
I/O ports (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through each V_{CC} or GND	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 3): DGG package	1 W
DL package	1.4 W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This value is limited to 4.6 V maximum.
 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V _{CC}	Supply voltage		2.3	3.6	V
V _{IH}	High-level input voltage	V _{CC} = 2.3 V to 2.7 V	1.7		V
		V _{CC} = 2.7 V to 3.6 V	2		
V _{IL}	Low-level input voltage	V _{CC} = 2.3 V to 2.7 V	0.7		V
		V _{CC} = 2.7 V to 3.6 V	0.8		
V _I	Input voltage		0	V _{CC}	V
V _O	Output voltage		0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2.3 V	−12		mA
		V _{CC} = 2.7 V	−12		
		V _{CC} = 3 V	−24		
I _{OL}	Low-level output current	V _{CC} = 2.3 V	12		mA
		V _{CC} = 2.7 V	12		
		V _{CC} = 3 V	24		
Δt/Δv	Input transition rise or fall rate		0	10	ns/V
T _A	Operating free-air temperature		−40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.



SN74ALVCH16270
12-BIT TO 24-BIT REGISTERED BUS EXCHANGER
WITH 3-STATE OUTPUTS

SCES028 – JULY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V _{CC} [†]	MIN	TYP [‡]	MAX	UNIT
V _{OH}	I _{OH} = −100 μA			MIN to MAX	V _{CC} −0.2			V
	I _{OH} = −6 mA, V _{IH} = 1.7 V			2.3 V	2			
	I _{OH} = −12 mA	V _{IH} = 1.7 V		2.3 V	1.7			
		V _{IH} = 2 V		2.7 V	2.2			
		V _{IH} = 2 V		3 V	2.4			
	I _{OH} = −24 mA, V _{IH} = 2 V			3 V	2			
V _{OL}	I _{OL} = 100 μA			MIN to MAX			0.2	V
	I _{OL} = 6 mA, V _{IL} = 0.7 V			2.3 V			0.4	
	I _{OL} = 12 mA	V _{IL} = 0.7 V		2.3 V			0.7	
		V _{IL} = 0.8 V		2.7 V			0.4	
	I _{OL} = 24 mA, V _{IL} = 0.8 V			3 V			0.55	
I _I	V _I = V _{CC} or GND			3.6 V			±5	μA
I _{I(hold)}	V _I = 0.7 V			2.3 V	45			μA
	V _I = 1.7 V		−45					
	V _I = 0.8 V			3 V	75			
	V _I = 2 V		−75					
	V _I = 0 to 3.6 V			3.6 V			±500	
I _{OZ} [§]	V _O = V _{CC} or GND			3.6 V			±10	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0			3.6 V			40	μA
ΔI _{CC}		One input at V _{CC} − 0.6 V, Other inputs at V _{CC} or GND		3 V to 3.6 V			750	μA
C _i	Control inputs	V _I = V _{CC} or GND		3.3 V	3.5			pF
C _{io}	A or B ports	V _O = V _{CC} or GND		3.3 V	9			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

‡ All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

§ For I/O ports, the parameter I_{OZ} includes the input leakage current.

SN74ALVCH16270

12-BIT TO 24-BIT REGISTERED BUS EXCHANGER

WITH 3-STATE OUTPUTS

SCES028 – JULY 1995

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

		$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	0	150	0	150	0	150	MHz
t_w	Pulse duration, CLK high or low	3.3		3.3		3.3		ns
t_{su}	A data before CLK \uparrow	4.1		3.8		3.1		ns
	B data before CLK \uparrow	0.9		1.2		0.9		
	$\overline{\text{CLKENA1}}$ or $\overline{\text{CLKENA2}}$ before CLK \uparrow	3.5		3.2		2.7		
	$\overline{\text{CLKEN1B}}$ or $\overline{\text{CLKEN2B}}$ before CLK \uparrow	3.4		3		2.6		
	$\overline{\text{OE}}$ data before CLK \uparrow	4.4		3.9		3.2		
t_h	A data after CLK \uparrow	0		0		0.2		ns
	B data after CLK \uparrow	1.4		1		1.7		
	$\overline{\text{CLKENA1}}$ or $\overline{\text{CLKENA2}}$ after CLK \uparrow	0		0.1		0.3		
	$\overline{\text{CLKEN1B}}$ or $\overline{\text{CLKEN2B}}$ after CLK \uparrow	0		0		0.6		
	$\overline{\text{OE}}$ after CLK \uparrow	0		0		0.1		

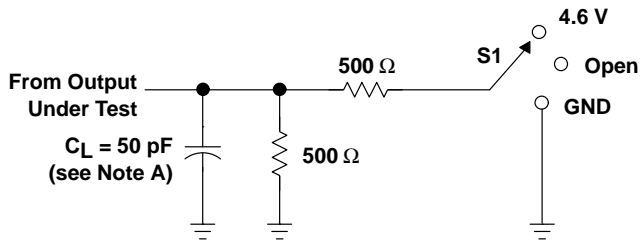
switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			150		150		150		MHz
t_{pd}	CLK	B	2	6.5	5.8		1.1	5.1	ns
	CLK	A	1.7	6	5.4		1	4.7	
	$\overline{\text{SEL}}$	A	1.9	6.8	6.4		1	5.5	
t_{en}	CLK	A or B	1.6	7.5	6.8		1	6	ns
t_{dis}	CLK	A or B	2.6	7.4	6.5		1.1	5.8	ns

operating characteristics, $T_A = 25^\circ\text{C}$

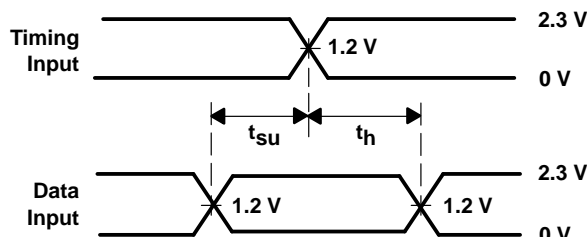
PARAMETER			TEST CONDITIONS	$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$	$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$	UNIT
				TYP	TYP	
C_{pd}	Power dissipation capacitance	Outputs enabled	$C_L = 50\text{ pF}$, $f = 10\text{ MHz}$	87	120	pF
		Outputs disabled		80.5	118	

PARAMETER MEASUREMENT INFORMATION
 $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$

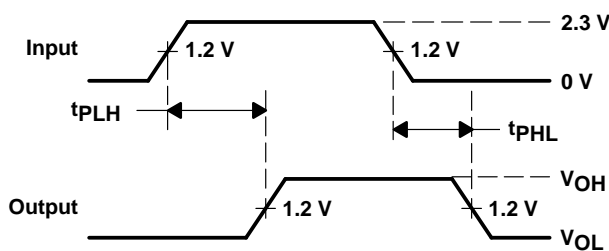


LOAD CIRCUIT

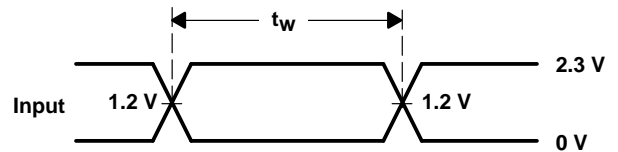
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	4.6 V
t_{PHZ}/t_{PZH}	GND



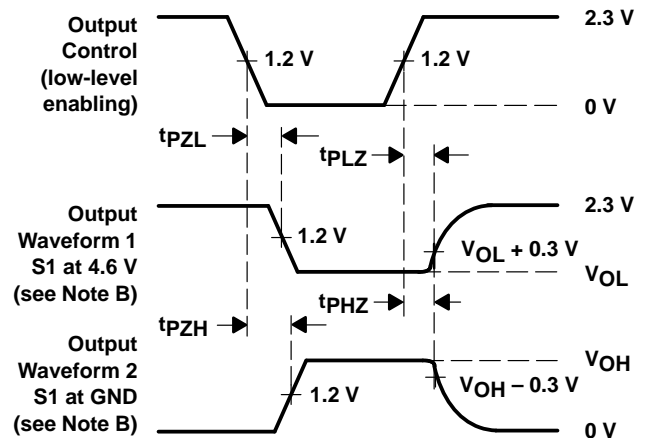
**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES**



**VOLTAGE WAVEFORMS
PULSE DURATION**



**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES**

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PHL} and t_{PLH} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

SN74ALVCH16270

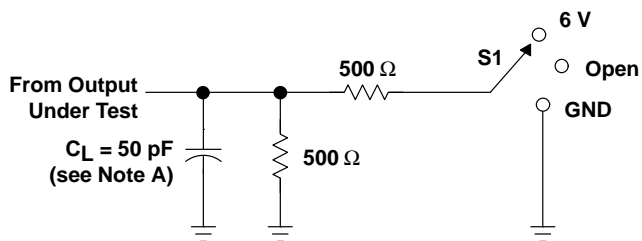
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SCES028 – JULY 1995

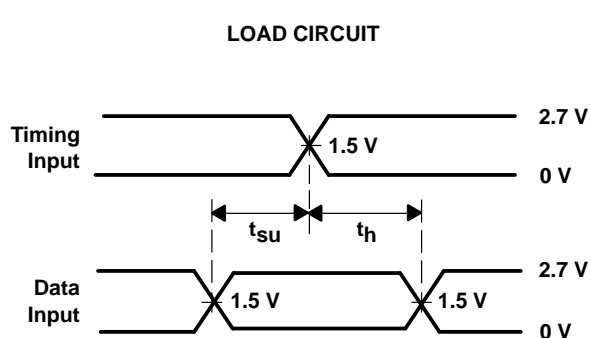
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$

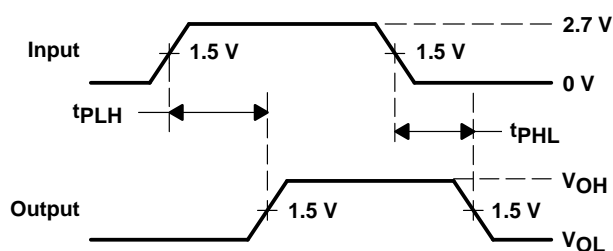


LOAD CIRCUIT

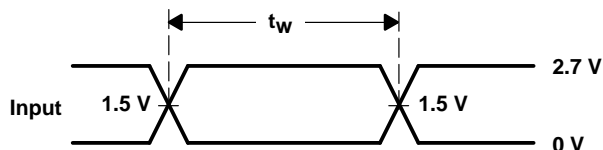
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



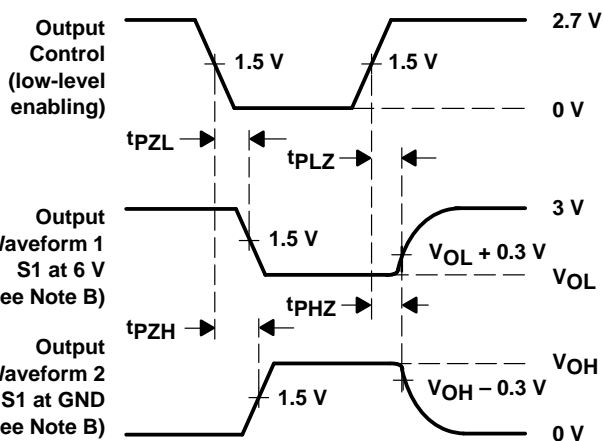
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
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 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PHL} and t_{PLH} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

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