

# SN74ALVCH16646

## 16-BIT BUS TRANSCEIVER AND REGISTER

### WITH 3-STATE OUTPUTS

SCES032A—JULY 1995—REVISED JUNE 1996

- Member of the Texas Instruments *Widebus™* Family
- *EPIC™* (Enhanced-Performance Implanted CMOS) Submicron Process
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

#### description

This 16-bit bus transceiver and register is designed for 2.3-V to 3.6-V  $V_{CC}$  operation.

The SN74ALVCH16646 can be used as two 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the SN74ALVCH16646.

Output-enable ( $\overline{OE}$ ) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. DIR determines which bus receives data when  $\overline{OE}$  is low. In the isolation mode ( $\overline{OE}$  high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, can be driven at a time.

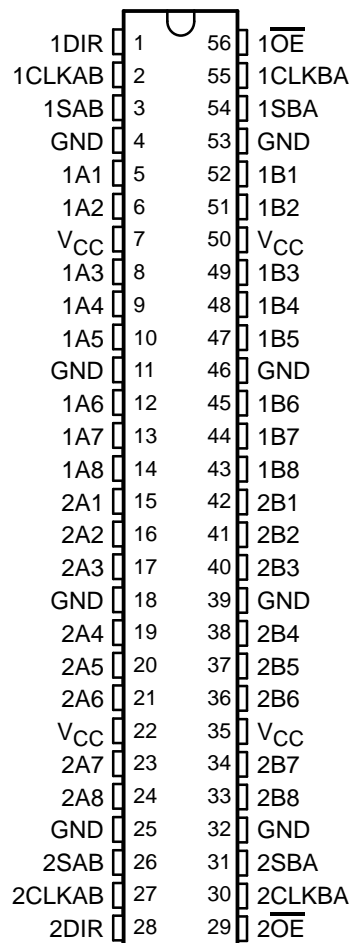
To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16646 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVCH16646 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

DGG OR DL PACKAGE  
(TOP VIEW)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1996, Texas Instruments Incorporated

# SN74ALVCH16646

## 16-BIT BUS TRANSCEIVER AND REGISTER

### WITH 3-STATE OUTPUTS

SCES032A—JULY 1995—REVISED JUNE 1996

FUNCTION TABLE

INPUTS						DATA I/Os		OPERATION OR FUNCTION
OE	DIR	CLKAB	CLKBA	SAB	SBA	A1 – A8	B1 – B8	
X	X	↑	X	X	X	Input	Unspecified†	Store A, B unspecified†
X	X	X	↑	X	X	Unspecified†	Input	Store B, A unspecified†
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	H or L	H or L	X	X	Input disabled	Input disabled	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time A data to B bus
L	H	H or L	X	H	X	Input	Output	Stored A data to B bus

† The data output functions may be enabled or disabled by various signals at the OE and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins is stored on every low-to-high transition of the clock inputs.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

**SN74ALVCH16646**  
**16-BIT BUS TRANSCEIVER AND REGISTER**  
**WITH 3-STATE OUTPUTS**

SCES032A—JULY 1995—REVISED JUNE 1996

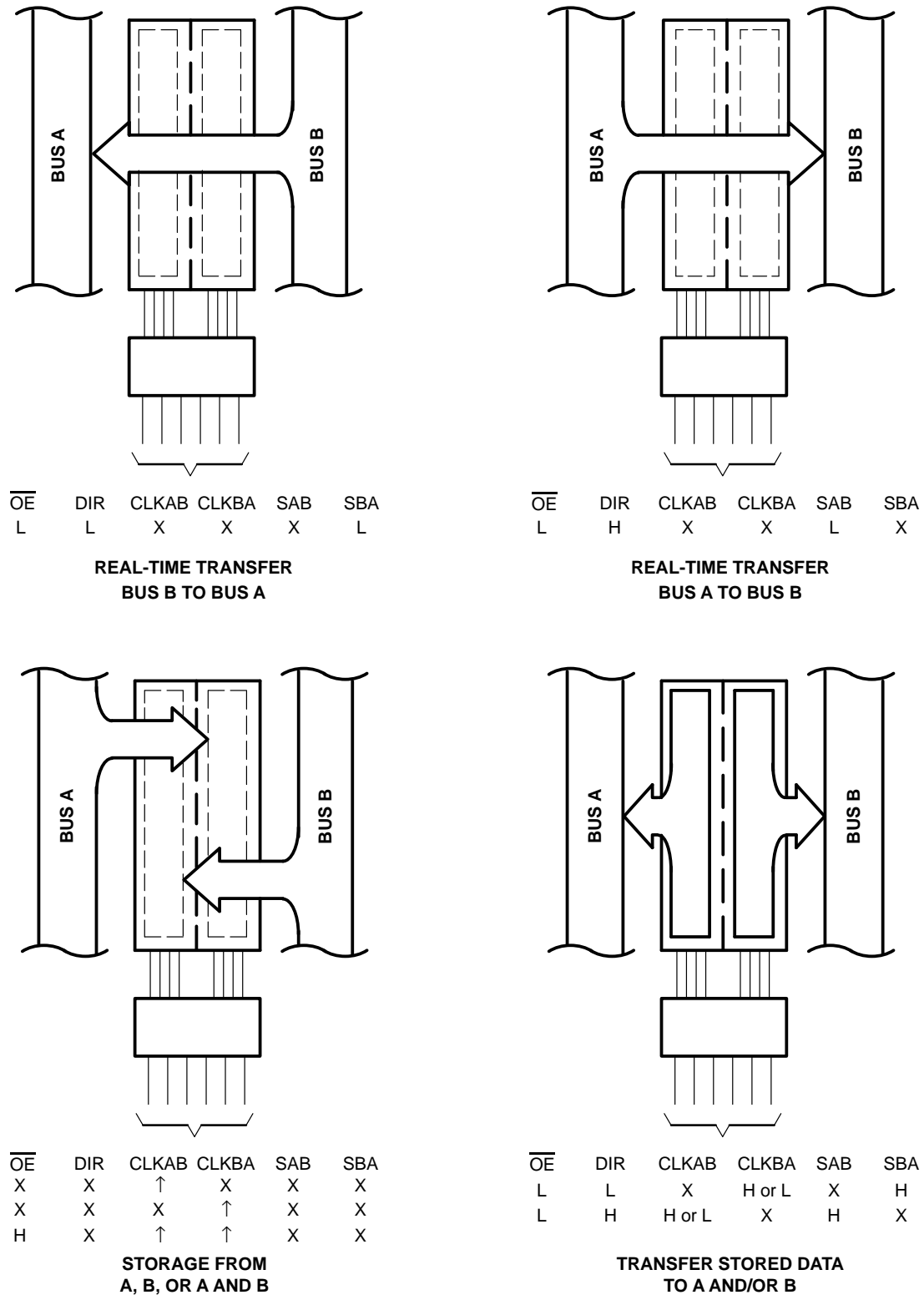


Figure 1. Bus-Management Functions

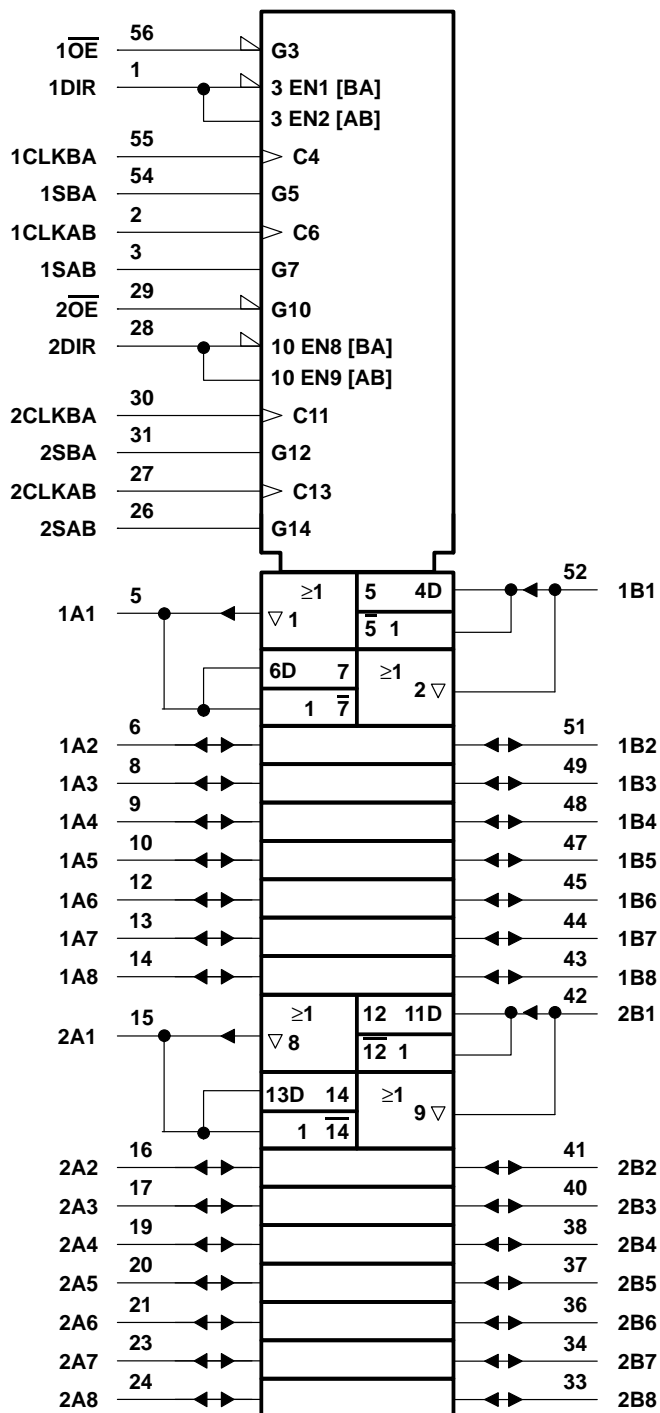
# SN74ALVCH16646

## 16-BIT BUS TRANSCEIVER AND REGISTER

### WITH 3-STATE OUTPUTS

SCES032A– JULY 1995 – REVISED JUNE 1996

logic symbol†

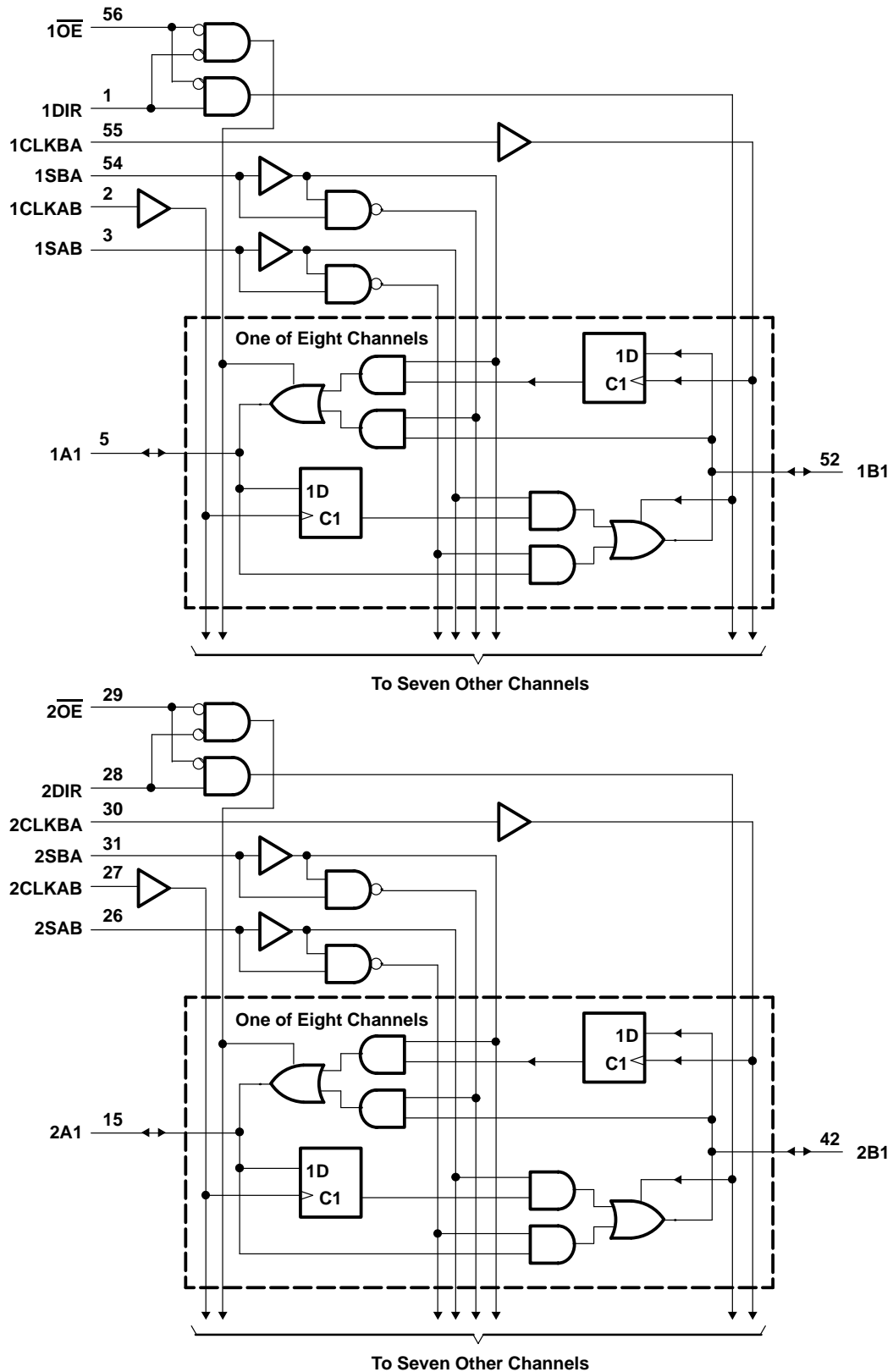


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

**SN74ALVCH16646**  
**16-BIT BUS TRANSCEIVER AND REGISTER**  
**WITH 3-STATE OUTPUTS**

SCES032A—JULY 1995—REVISED JUNE 1996

logic diagram (positive logic)



# SN74ALVCH16646

## 16-BIT BUS TRANSCEIVER AND REGISTER

### WITH 3-STATE OUTPUTS

SCES032A– JULY 1995 – REVISED JUNE 1996

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	–0.5 V to 4.6 V
Input voltage range, $V_I$ : Except I/O ports (see Note 1)	–0.5 V to 4.6 V
I/O ports (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, $V_O$ (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±50 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±50 mA
Continuous current through each $V_{CC}$ or GND	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 3): DGG package	1 W
DL package	1.4 W
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. This value is limited to 4.6 V maximum.  
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*.

#### recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		2.3	3.6	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2.3 V to 2.7 V	1.7		V
		V <sub>CC</sub> = 2.7 V to 3.6 V	2		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2.3 V to 2.7 V	0.7		V
		V <sub>CC</sub> = 2.7 V to 3.6 V	0.8		
V <sub>I</sub>	Input voltage		0	V <sub>CC</sub>	V
V <sub>O</sub>	Output voltage		0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 2.3 V	−12		mA
		V <sub>CC</sub> = 2.7 V	−12		
		V <sub>CC</sub> = 3 V	−24		
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 2.3 V	12		mA
		V <sub>CC</sub> = 2.7 V	12		
		V <sub>CC</sub> = 3 V	24		
Δt/Δv	Input transition rise or fall rate		0	10	ns/V
T <sub>A</sub>	Operating free-air temperature		−40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.



**SN74ALVCH16646**  
**16-BIT BUS TRANSCEIVER AND REGISTER**  
**WITH 3-STATE OUTPUTS**

SCES032A– JULY 1995 – REVISED JUNE 1996

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	V <sub>CC</sub> <sup>†</sup>	MIN	TYP <sup>‡</sup>	MAX	UNIT
V <sub>OH</sub>	I <sub>OH</sub> = −100 μA		MIN to MAX	V <sub>CC</sub> − 0.2			V
	I <sub>OH</sub> = −6 mA, V <sub>IH</sub> = 1.7 V		2.3 V	2			
	I <sub>OH</sub> = −12 mA	V <sub>IH</sub> = 1.7 V	2.3 V	1.7			
		V <sub>IH</sub> = 2 V	2.7 V	2.2			
		V <sub>IH</sub> = 2 V	3 V	2.4			
	I <sub>OH</sub> = −24 mA, V <sub>IH</sub> = 2 V		3 V	2			
V <sub>OL</sub>	I <sub>OL</sub> = 100 μA		MIN to MAX			0.2	V
	I <sub>OL</sub> = 6 mA, V <sub>IL</sub> = 0.7 V		2.3 V			0.4	
	I <sub>OL</sub> = 12 mA	V <sub>IL</sub> = 0.7 V	2.3 V			0.7	
		V <sub>IL</sub> = 0.8 V	2.7 V			0.4	
	I <sub>OL</sub> = 24 mA, V <sub>IL</sub> = 0.8 V		3 V			0.55	
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND		3.6 V			±5	μA
I <sub>I</sub> (hold)	V <sub>I</sub> = 0.7 V		2.3 V	45			μA
	V <sub>I</sub> = 1.7 V			−45			
	V <sub>I</sub> = 0.8 V		3 V	75			
	V <sub>I</sub> = 2 V			−75			
	V <sub>I</sub> = 0 to 3.6 V <sup>§</sup>		3.6 V			±500	
I <sub>OZ</sub> <sup>¶</sup>	V <sub>O</sub> = V <sub>CC</sub> or GND		3.6 V			±10	μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0		3.6 V			40	μA
ΔI <sub>CC</sub>	One input at V <sub>CC</sub> − 0.6 V, Other inputs at V <sub>CC</sub> or GND		3 V to 3.6 V			750	μA
C <sub>i</sub>	Control inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V	3.5			pF
C <sub>io</sub>	A or B ports	V <sub>O</sub> = V <sub>CC</sub> or GND	3.3 V	8.5			pF

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

<sup>‡</sup> Typical values are measured at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

<sup>§</sup> This is the bus-hold maximum dynamic current required to switch the input from one state to another.

<sup>¶</sup> For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.

**timing requirements over recommended operating free-air temperature range (unless otherwise noted)**

			V <sub>CC</sub> = 2.5 V ±0.2 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ±0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency		0	150	0	150	0	150	MHz
t <sub>w</sub>	Pulse duration	CLKAB or CLKBA high or low	3.3		3.3		3.3		ns
t <sub>su</sub>	Setup time	A before CLKAB↑ or B before CLKBA↑	1.6		1.7		1.4		ns
t <sub>h</sub>	Hold time	A after CLKAB↑ or B after CLKBA↑	0.6		0.4		0.7		ns



# SN74ALVCH16646

## 16-BIT BUS TRANSCEIVER AND REGISTER

### WITH 3-STATE OUTPUTS

SCES032A– JULY 1995 – REVISED JUNE 1996

switching characteristics over recommended operating free-air temperature range,  $C_L = 50$  pF (unless otherwise noted) (see Figures 2 and 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$f_{max}$			150		150		150		MHz
$t_{pd}$	A or B	B or A	1	5.4	4.5		1	3.9	ns
	CLKAB or CLKBA	A or B	1	6.2	5.2		1	4.5	
	SAB or SBA	A or B	1	7.4	6.4		1	5.3	
$t_{en}$	$\overline{OE}$	A or B	1	7	6.2		1	5.1	ns
$t_{dis}$	$\overline{OE}$	A or B	1.8	5.9	5		1.4	4.7	ns
$t_{en}$	DIR	A or B	1	8.3	6.2		1	5.1	ns
$t_{dis}$	DIR	A or B	1.7	6.7	6		1.1	5.3	ns

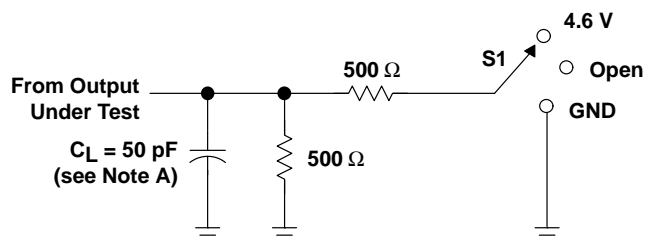
operating characteristics,  $T_A = 25^\circ\text{C}$

PARAMETER			TEST CONDITIONS	V <sub>CC</sub> = 2.5 V ± 0.2 V	V <sub>CC</sub> = 3.3 V ± 0.3 V	UNIT
				TYP	TYP	
C <sub>pd</sub>	Power dissipation capacitance	Outputs enabled	C <sub>L</sub> = 50 pF, f = 10 MHz	39	43	pF
		Outputs disabled		10	12	



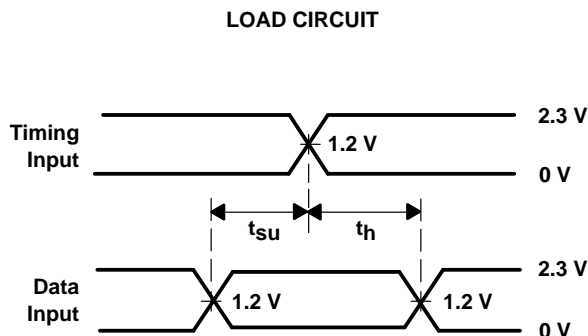
## PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

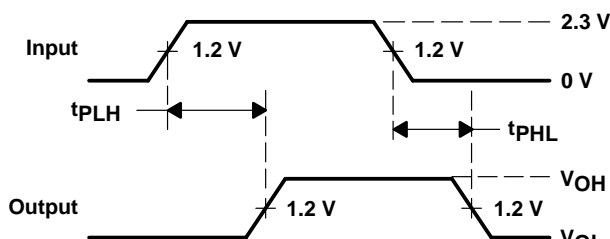


**LOAD CIRCUIT**

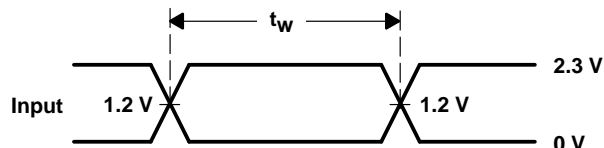
TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	4.6 V
$t_{PHZ}/t_{PZH}$	GND



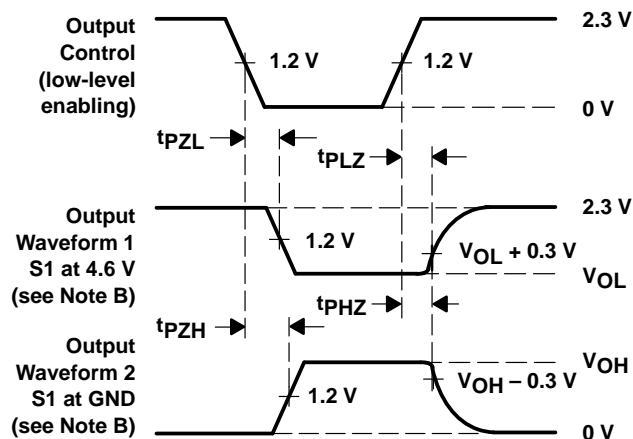
**VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES**



**VOLTAGE WAVEFORMS  
PULSE DURATION**



**VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES**

- NOTES: A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
- D. The outputs are measured one at a time with one transition per measurement.
- E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

**Figure 2. Load Circuit and Voltage Waveforms**

# SN74ALVCH16646

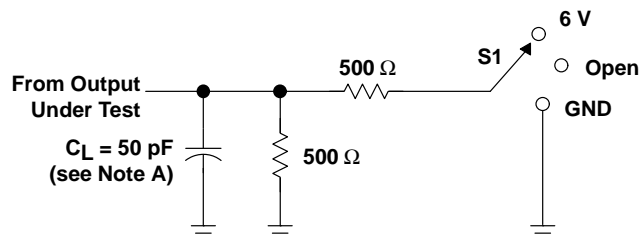
## 16-BIT BUS TRANSCEIVER AND REGISTER

### WITH 3-STATE OUTPUTS

SCES032A—JULY 1995—REVISED JUNE 1996

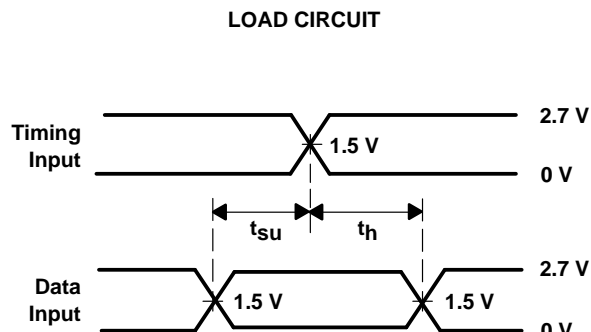
#### PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$

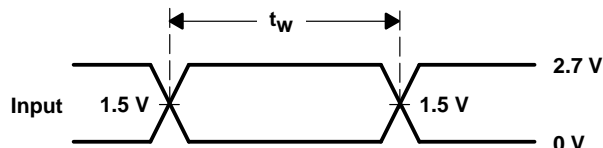


LOAD CIRCUIT

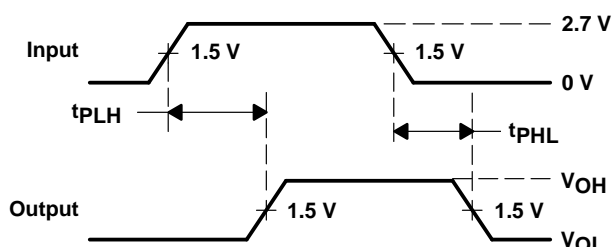
TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND



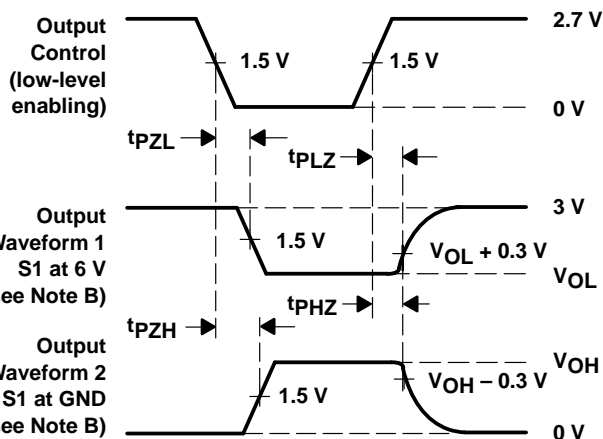
VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\text{ }\Omega$ ,  $t_r \leq 2.5\text{ ns}$ ,  $t_f \leq 2.5\text{ ns}$ .
  - The outputs are measured one at a time with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 3. Load Circuit and Voltage Waveforms

## **IMPORTANT NOTICE**

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

**TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.**

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.