

SN74ALVCH16652 16-BIT BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

SCES034 – JULY 1995

- Member of the Texas Instruments *Widebus™* Family
- *EPIC™* (Enhanced-Performance Implanted CMOS) Submicron Process
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 16-bit bus transceiver and register is designed for 2.3-V to 3.6-V V_{CC} operation.

The SN74ALVCH16652 consists of D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. The device can be used as two 8-bit transceivers or one 16-bit transceiver.

Complementary output-enable (OEAB and \overline{OEBA}) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. A low input level selects real-time data, and a high input level selects stored data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the SN74ALVCH16652.

Data on the A or B bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) inputs regardless of the levels on the select-control or output-enable inputs. When SAB and SBA are in the real-time transfer mode, it also is possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and \overline{OEBA} . In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus line are in the high-impedance state, each set of bus lines remains at its last level configuration.

Active bus-hold circuitry is provided to hold unused for floating inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, \overline{OEBA} should be tied to V_{CC} through a pullup resistor and OEAB should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking current-sourcing capability of the driver.

The SN74ALVCH16652 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVCH16652 is characterized for operation from -40°C to 85°C .



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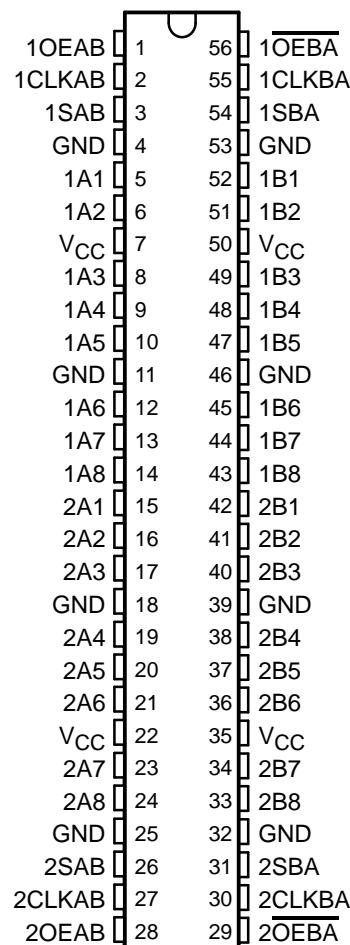
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DGG OR DL PACKAGE (TOP VIEW)



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FUNCTION TABLE

INPUTS						DATA I/O†		OPERATION OR FUNCTION
OEAB	OEBA	CLKAB	CLKBA	SAB	SBA	A1 – A8	B1 – B8	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B data
X	H	↑	H or L	X	X	Input	Unspecified‡	Store A, hold B
H	H	↑	↑	X‡	X	Input	Output	Store A in both registers
L	X	H or L	↑	X	X	Unspecified‡	Input	Hold A, store B
L	L	↑	↑	X	X‡	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
H	H	X	X	L	X	Input	Output	Real-time A data to B bus
H	H	H or L	X	H	X	Input	Output	Stored A data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored A data to B bus and stored B data to A bus

† The data output functions may be enabled or disabled by a variety of level combinations at the OEAB or OEBA inputs. Data input functions are always enabled; i.e., data at the bus pins is stored on every low-to-high transition of the clock inputs.

‡ Select control = L; clocks can occur simultaneously
Select control = H; clocks must be staggered in order to load both registers

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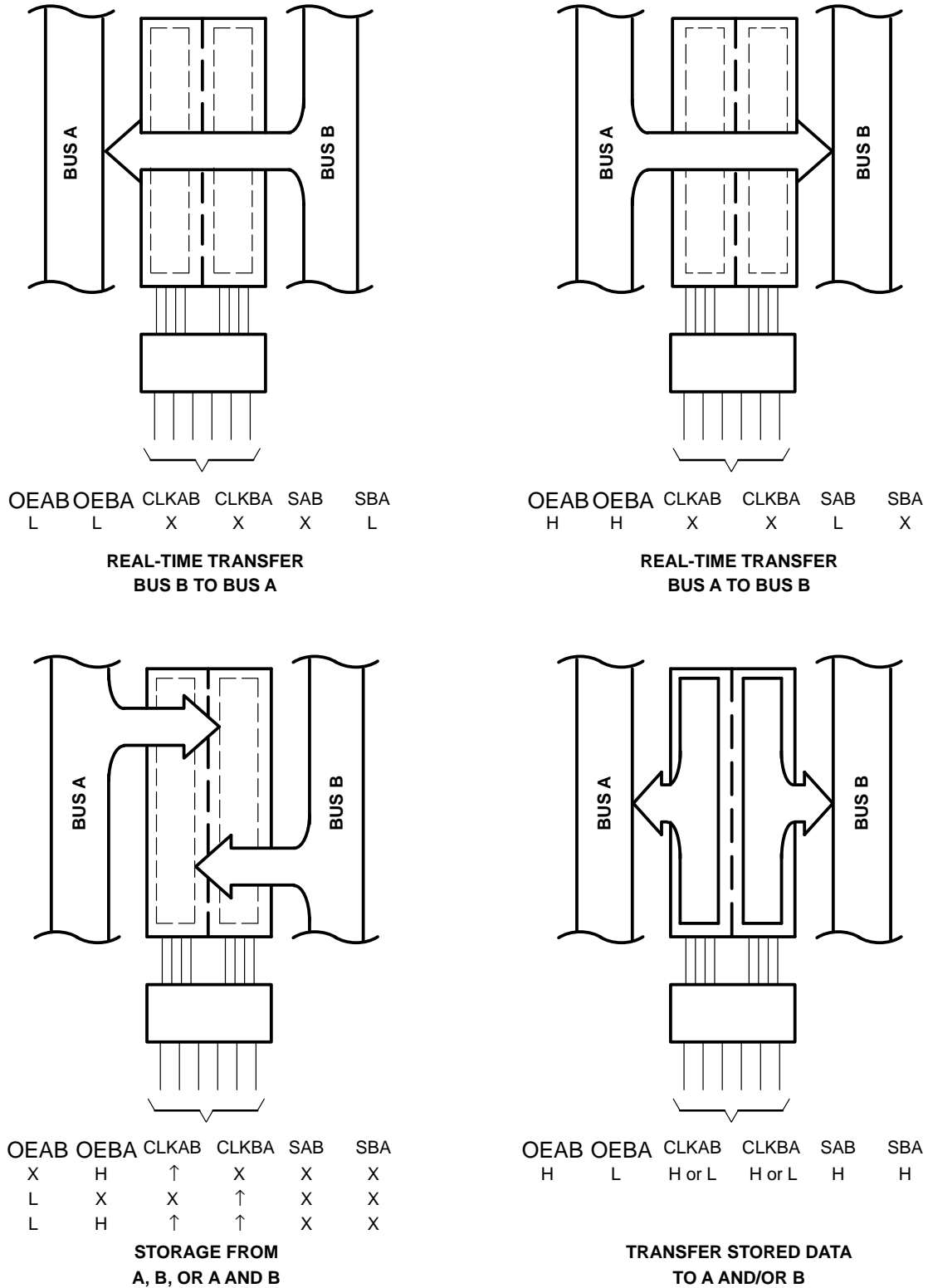


Figure 1. Bus-Management Functions

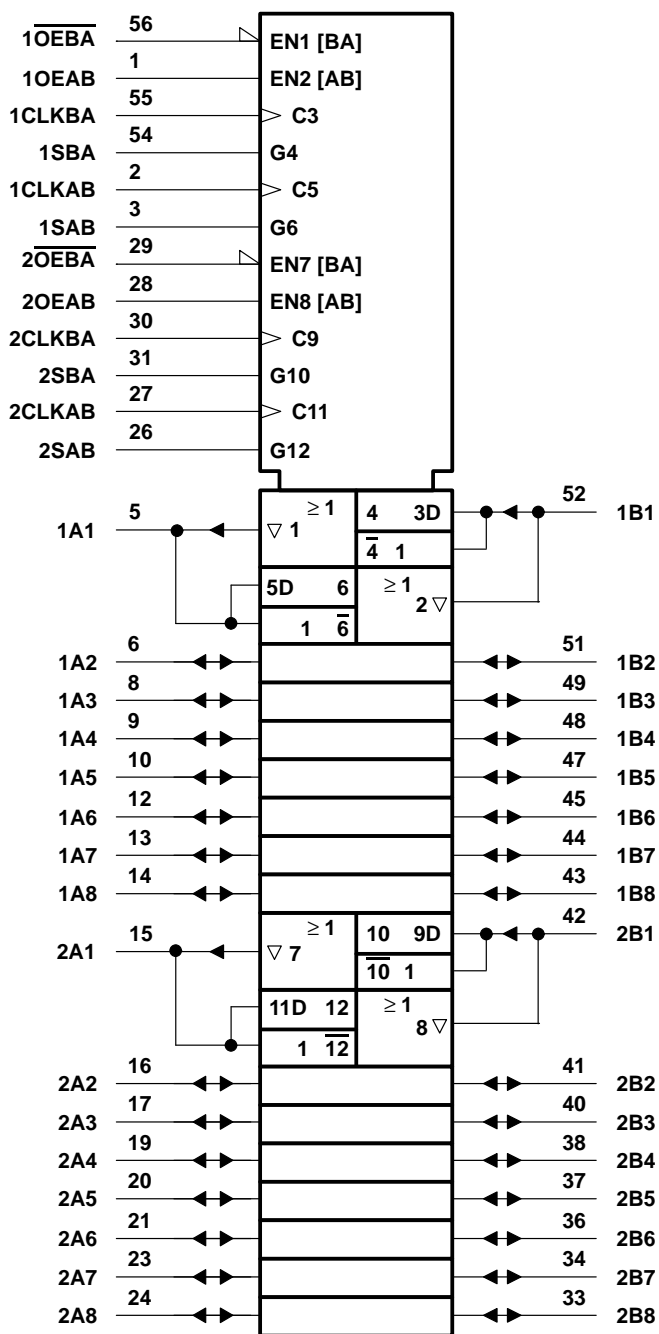
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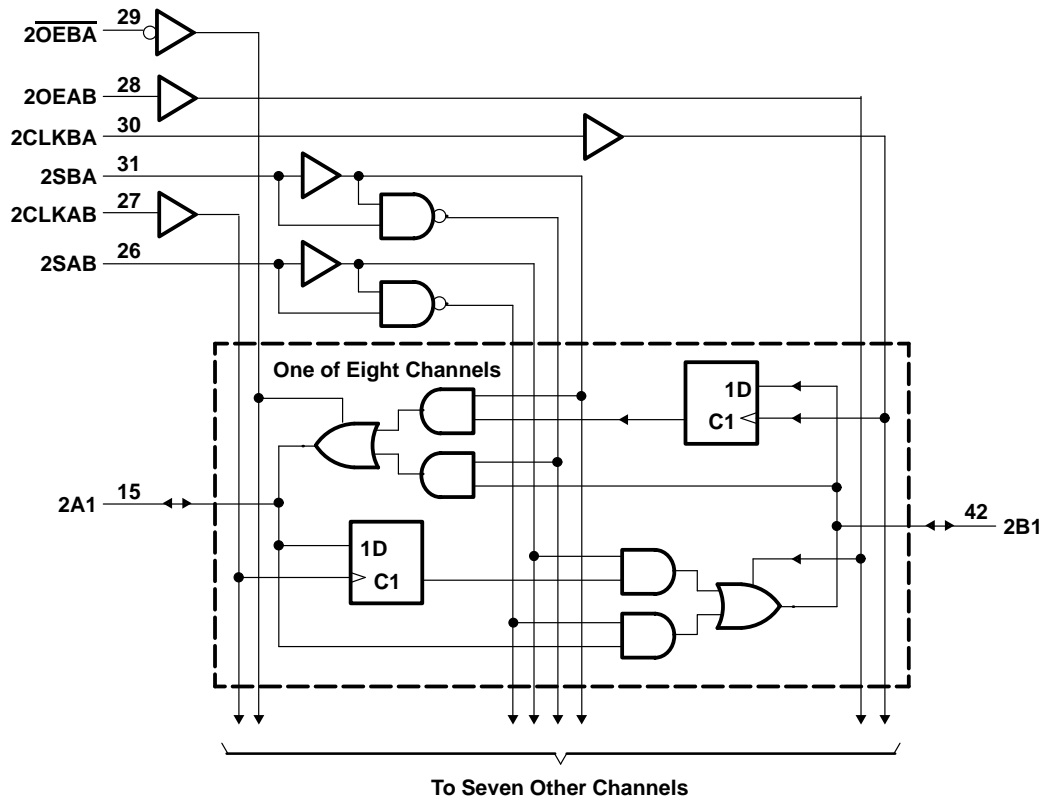
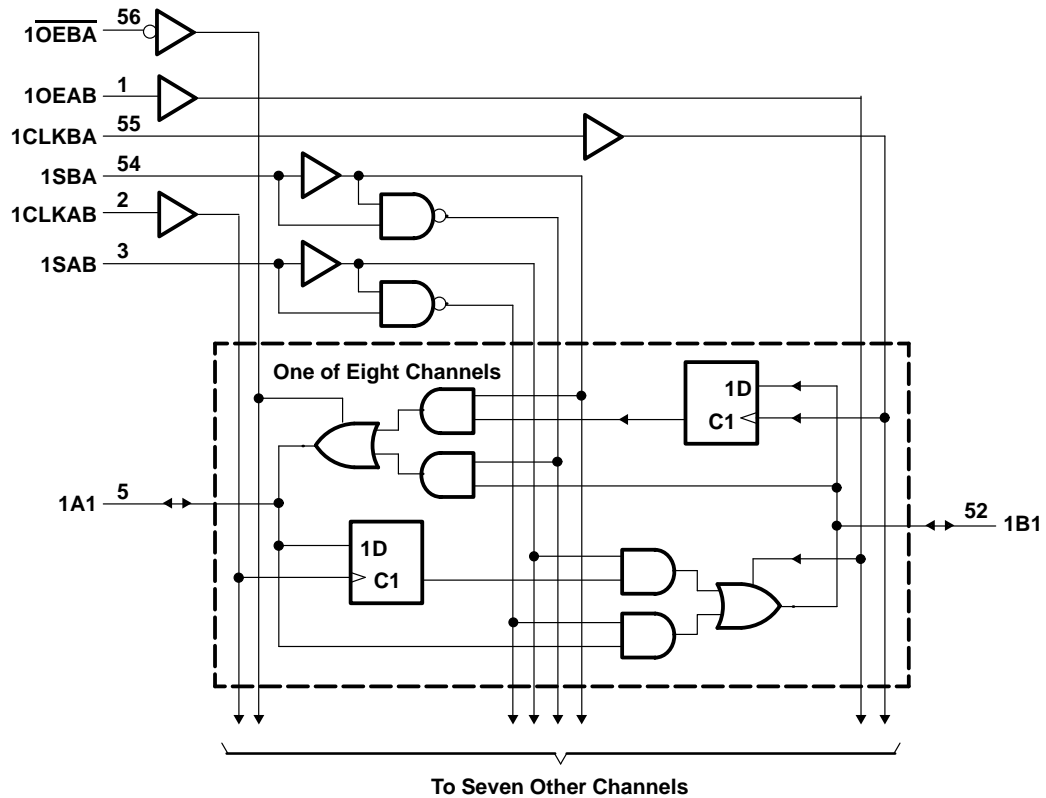
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I : Except I/O ports (see Note 1)	–0.5 V to 4.6 V
I/O ports (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through each V_{CC} or GND	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 3): DGG package	1 W
DL package	1.4 W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This value is limited to 4.6 V maximum.
 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V _{CC}	Supply voltage		2.3	3.6	V
V _{IH}	High-level input voltage	V _{CC} = 2.3 V to 2.7 V	1.7		V
		V _{CC} = 2.7 V to 3.6 V	2		
V _{IL}	Low-level input voltage	V _{CC} = 2.3 V to 2.7 V	0.7		V
		V _{CC} = 2.7 V to 3.6 V	0.8		
V _I	Input voltage		0	V _{CC}	V
V _O	Output voltage		0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2.3 V	−12		mA
		V _{CC} = 2.7 V	−12		
		V _{CC} = 3 V	−24		
I _{OL}	Low-level output current	V _{CC} = 2.3 V	12		mA
		V _{CC} = 2.7 V	12		
		V _{CC} = 3 V	24		
Δt/Δv	Input transition rise or fall rate		0	10	ns/V
T _A	Operating free-air temperature		−40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V _{CC} [†]	MIN	TYP [‡]	MAX	UNIT
V _{OH}	I _{OH} = −100 μA			MIN to MAX	V _{CC} − 0.2			V
	I _{OH} = −6 mA, V _{IH} = 1.7 V			2.3 V	2			
	I _{OH} = −12 mA	V _{IH} = 1.7 V		2.3 V	1.7			
		V _{IH} = 2 V		2.7 V	2.2			
		V _{IH} = 2 V		3 V	2.4			
	I _{OH} = −24 mA, V _{IH} = 2 V			3 V	2			
V _{OL}	I _{OL} = 100 μA			MIN to MAX			0.2	V
	I _{OL} = 6 mA, V _{IL} = 0.7 V			2.3 V			0.4	
	I _{OL} = 12 mA	V _{IL} = 0.7 V		2.3 V			0.7	
		V _{IL} = 0.8 V		2.7 V			0.4	
	I _{OL} = 24 mA, V _{IL} = 0.8 V			3 V			0.55	
I _I	V _I = V _{CC} or GND			3.6 V			±5	μA
I _I (hold)	V _I = 0.7 V			2.3 V	45			μA
	V _I = 1.7 V		−45					
	V _I = 0.8 V			3 V	75			
	V _I = 2 V		−75					
	V _I = 0 to 3.6 V			3.6 V	±500			
I _{OZ} [§]	V _O = V _{CC} or GND			3.6 V			±10	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0			3.6 V			40	μA
ΔI _{CC}		One input at V _{CC} − 0.6 V, Other inputs at V _{CC} or GND		3 V to 3.6 V		750		μA
C _i	Control inputs	V _I = V _{CC} or GND		3.3 V				pF
C _{io}	A or B ports	V _O = V _{CC} or GND		3.3 V				pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

[‡] Typical values are measured at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^\circ \text{C}$.

[§] For I/O ports, the parameter I_{OZ} includes the input leakage current.

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