

# SN74ALVCH16272

## 12-BIT TO 24-BIT MULTIPLEXED BUS EXCHANGER

### WITH 3-STATE OUTPUTS

SCES057 – OCTOBER 1995

- Member of the Texas Instruments **Widebus™** Family
- **EPIC™** (Enhanced-Performance Implanted CMOS) Submicron Process
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Packaged in Plastic Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

#### description

This 12-bit to 24-bit bus exchanger is designed for 2.3-V to 3.3-V  $V_{CC}$  operation.

The SN74ALVCH16272 is intended for applications where two separate datapaths must be multiplexed onto, or demultiplexed from, a single datapath. This device is particularly suitable as an interface between conventional DRAMs and high-speed microprocessors.

Data from the A inputs is stored in the internal registers on the low-to-high transition of the clock (CLK) input, when the  $\overline{CLKENA}$  inputs are low. A two-stage pipeline is provided in each of the A-to-1B and A-to-2B paths to serve as a shallow write buffer.

Transparent latches are provided in the B-to-A path to allow asynchronous operation to maximize memory access throughput. These latches transfer data when the latch-enable ( $\overline{LE}$ ) inputs are low. The select ( $\overline{SEL}$ ) line selects 1B or 2B data for the A outputs. Data flow is controlled by the active-low output enables ( $\overline{OE_A}$ ,  $\overline{OE_B}$ ).

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16272 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVCH16272 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

DGG OR DL PACKAGE  
(TOP VIEW)

$\overline{OE_A}$	1	56	$\overline{OE_B}$
$\overline{LE_{1B}}$	2	55	$\overline{CLKENA_2}$
2B3	3	54	2B4
GND	4	53	GND
2B2	5	52	2B5
2B1	6	51	2B6
$V_{CC}$	7	50	$V_{CC}$
A1	8	49	2B7
A2	9	48	2B8
A3	10	47	2B9
GND	11	46	GND
A4	12	45	2B10
A5	13	44	2B11
A6	14	43	2B12
A7	15	42	1B12
A8	16	41	1B11
A9	17	40	1B10
GND	18	39	GND
A10	19	38	1B9
A11	20	37	1B8
A12	21	36	1B7
$V_{CC}$	22	35	$V_{CC}$
1B1	23	34	1B6
1B2	24	33	1B5
GND	25	32	GND
1B3	26	31	1B4
$\overline{LE_{2B}}$	27	30	$\overline{CLKENA_1}$
$\overline{SEL}$	28	29	CLK

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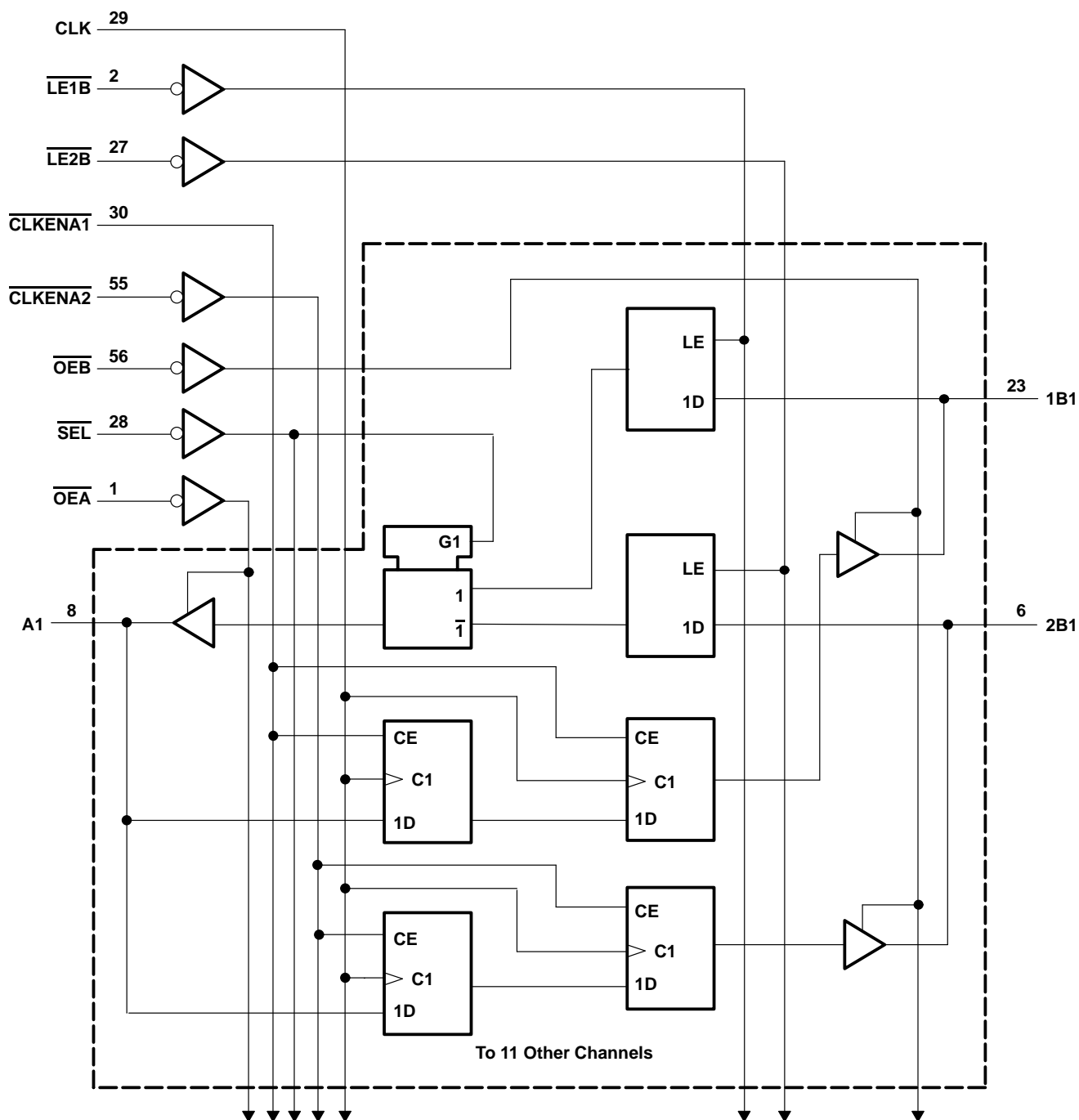
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logic diagram (positive logic)



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### Function Tables

#### OUTPUT ENABLE

INPUTS		OUTPUTS	
$\overline{\text{OEA}}$	$\overline{\text{OEB}}$	A	1B, 2B
H	H	Z	Z
H	L	Z	Active
L	H	Active	Z
L	L	Active	Active

#### A-TO-B STORAGE ( $\overline{\text{OEB}} = \text{L}$ )

INPUTS				OUTPUTS	
$\overline{\text{CLKENA1}}$	$\overline{\text{CLKENA2}}$	CLK	A	1B	2B
H	H	X	X	1B <sub>0</sub> <sup>†</sup>	2B <sub>0</sub> <sup>†</sup>
L	X	↑	L	L <sup>†</sup>	X
L	X	↑	H	H <sup>†</sup>	X
X	L	↑	L	X	L
X	L	↑	H	A <sub>0</sub>	H

† Two CLK edges are needed to propagate data.

#### B-TO-A STORAGE ( $\overline{\text{OEA}} = \text{L}$ )

INPUTS				OUTPUT A
$\overline{\text{LE}}$	$\overline{\text{SEL}}$	1B	2B	
H	X	X	X	A <sub>0</sub> <sup>‡</sup>
H	X	X	X	A <sub>0</sub> <sup>‡</sup>
L	H	L	X	L
L	H	H	X	H
L	L	X	L	L
L	L	X	H	H

‡ Output level before the indicated steady-state input conditions were established

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#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	–0.5 V to 4.6 V
Input voltage range, $V_I$ : Except I/O ports (see Note 1)	–0.5 V to 4.6 V
I/O ports (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, $V_O$ (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±50 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±50 mA
Continuous current through each $V_{CC}$ or GND	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 3): DGG package	1 W
DL package	1.4 W
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
 2. This value is limited to 4.6 V maximum.  
 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

#### recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		2.3	3.6	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2.3 V to 2.7 V	1.7		V
		V <sub>CC</sub> = 2.7 V to 3.6 V	2		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2.3 V to 2.7 V	0.7		V
		V <sub>CC</sub> = 2.7 V to 3.6 V	0.8		
V <sub>I</sub>	Input voltage		0	V <sub>CC</sub>	V
V <sub>O</sub>	Output voltage		0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 2.3 V	−12		mA
		V <sub>CC</sub> = 2.7 V	−12		
		V <sub>CC</sub> = 3 V	−24		
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 2.3 V	12		mA
		V <sub>CC</sub> = 2.7 V	12		
		V <sub>CC</sub> = 3 V	24		
Δt/Δv	Input transition rise or fall rate		0	10	ns/V
T <sub>A</sub>	Operating free-air temperature		−40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V <sub>CC</sub> <sup>†</sup>	MIN	TYP <sup>‡</sup>	MAX	UNIT
V <sub>OH</sub>	I <sub>OH</sub> = −100 μA		MIN to MAX	V <sub>CC</sub> − 0.2			V
	I <sub>OH</sub> = −6 mA, V <sub>IH</sub> = 1.7 V		2.3 V	2			
	I <sub>OH</sub> = −12 mA	V <sub>IH</sub> = 1.7 V	2.3 V	1.7			
		V <sub>IH</sub> = 2 V	2.7 V	2.2			
		V <sub>IH</sub> = 2 V	3 V	2.4			
	I <sub>OH</sub> = −24 mA, V <sub>IH</sub> = 2 V		3 V	2			
V <sub>OL</sub>	I <sub>OL</sub> = 100 μA		MIN to MAX			0.2	V
	I <sub>OL</sub> = 6 mA, V <sub>IL</sub> = 0.7 V		2.3 V			0.4	
	I <sub>OL</sub> = 12 mA	V <sub>IL</sub> = 0.7 V	2.3 V			0.7	
		V <sub>IL</sub> = 0.8 V	2.7 V			0.4	
	I <sub>OL</sub> = 24 mA, V <sub>IL</sub> = 0.8 V		3 V			0.55	
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND		3.6 V			±5	μA
I <sub>I</sub> (hold)	V <sub>I</sub> = 0.7 V		2.3 V	45			μA
	V <sub>I</sub> = 1.7 V			−45			
	V <sub>I</sub> = 0.8 V		3 V	75			
	V <sub>I</sub> = 2 V			−75			
	V <sub>I</sub> = 0 to 3.6 V		3.6 V			±500	
I <sub>OZ</sub> <sup>§</sup>	V <sub>O</sub> = V <sub>CC</sub> or GND		3.6 V			±10	μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0		3.6 V			40	μA
ΔI <sub>CC</sub>	One input at V <sub>CC</sub> − 0.6 V, Other inputs at V <sub>CC</sub> or GND		3 V to 3.6 V			750	μA
C <sub>i</sub>	Control inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V				pF
C <sub>io</sub>	A or B ports	V <sub>O</sub> = V <sub>CC</sub> or GND	3.3 V				pF

$^{\dagger}$  For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

$^{\ddagger}$  Typical values are measured at  $V_{CC} = 3.3 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

$^{\S}$  For I/O ports, the parameter  $I_{OZ}$  includes the input leakage current.

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