

SN74LVC16244A

16-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS

SCES061A – DECEMBER 1995 – REVISED JANUARY 1996

- Member of the Texas Instruments *Widebus™* Family
- *EPIC™* (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce)
< 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot)
> 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Supports Mixed-Mode Signal Operation
(5-V Input/Output Voltage With 3.3-V V_{CC})
- ESD Protection Exceeds 2000 V Per
MIL-STD-883C, Method 3015; Exceeds
200 V Using Machine Model
(C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA
Per JEDEC Standard JESD-17
- Package Options Include Plastic 300-mil
Shrink Small-Outline (DL) and Thin Shrink
Small-Outline (DGG) Packages

description

This 16-bit buffer/driver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC16244A is designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

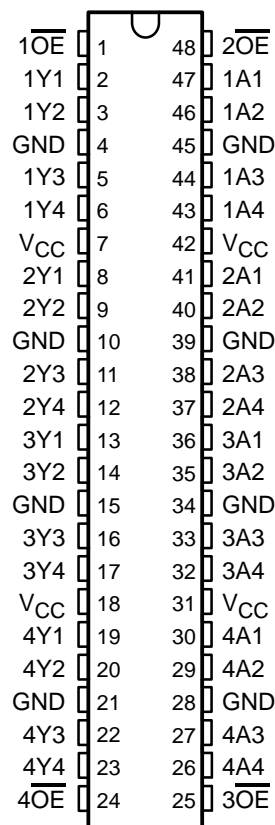
The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. It provides true outputs and symmetrical active-low output-enable (\overline{OE}) inputs.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

The SN74LVC16244A is characterized for operation from -40°C to 85°C .

DGG OR DL PACKAGE
(TOP VIEW)



FUNCTION TABLE
(each 4-bit buffer)

INPUTS		OUTPUT
\overline{OE}	A	Y
L	H	H
L	L	L
H	X	Z



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**TEXAS
INSTRUMENTS**

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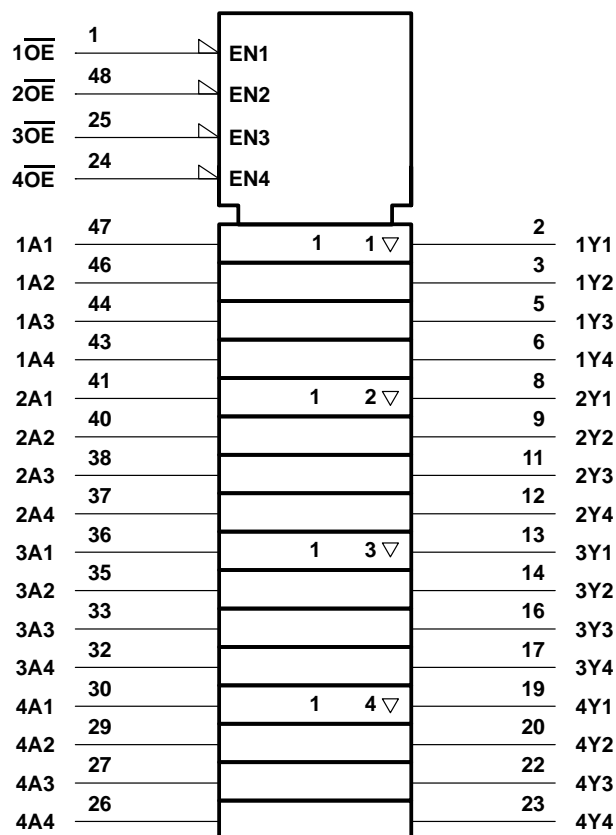
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16-BIT BUFFER/DRIVER

WITH 3-STATE OUTPUTS

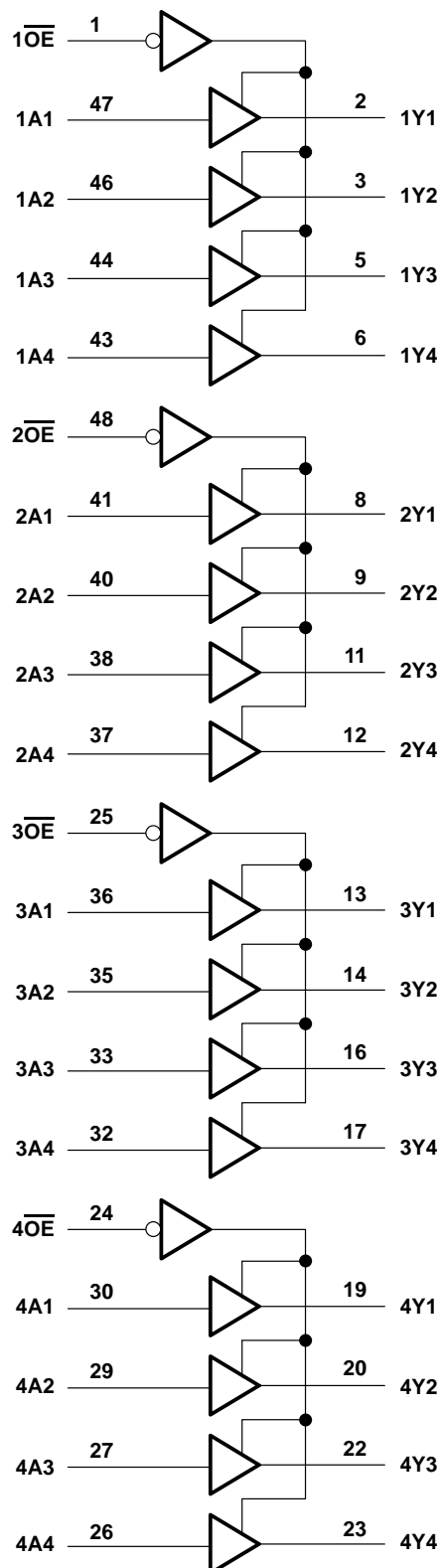
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I (see Note 1)	–0.5 V to 6.5 V
Voltage applied to any output in the high-impedance state or power-off state, V_O (see Note 1)	–0.5 V to 6.5 V
Voltage applied to any output in the high or low state, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through each V_{CC} or GND	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 3): DGG package	0.85 W
DL package	1.2 W
Operating free-air temperature range, T_A	–40°C to 85°C
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V_{CC}	Supply voltage	Operating	2	3.6	V
		Data retention only	1.5		
V_{IH}	High-level input voltage	$V_{CC} = 2.7$ V to 3.6 V	2		V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		0.8	V
V_I	Input voltage		0	5.5	V
V_O	Output voltage	High or low state	0	V_{CC}	V
		3 state	0	5.5	
I_{OH}	High-level output current	$V_{CC} = 2.7$ V		–12	mA
		$V_{CC} = 3$ V		–24	
I_{OL}	Low-level output current	$V_{CC} = 2.7$ V		12	mA
		$V_{CC} = 3$ V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		–40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC} [†]	MIN	TYP [‡]	MAX	UNIT
V _{OH}	I _{OH} = –100 µA	MIN to MAX	V _{CC} – 0.2			V
	I _{OH} = –12 mA	2.7 V	2			
	I _{OH} = –12 mA	3 V	2.2			
	I _{OH} = –24 mA	3 V	2			
V _{OL}	I _{OL} = 100 µA	MIN to MAX	0.2			V
	I _{OL} = 12 mA	2.7 V	0.4			
	I _{OL} = 24 mA	3 V	0.55			
I _I	V _I = 5.5 V or GND	3.6 V	±5			µA
I _{off}	V _I or V _O = 5.5 V	0	50			µA
I _{OZ}	V _O = 0 to 5.5 V	3.6 V	±20			µA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V	20			µA
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	3 V to 3.6 V	500			µA
C _i	V _I = V _{CC} or GND	3.3 V	4.7			pF
C _o	V _O = V _{CC} or GND	3.3 V	6.1			pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

[‡] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	
t _{pd}	A	Y	1.5	5.2		5.8	ns
t _{en}	$\overline{\text{OE}}$	Y	1.5	7.5		8.2	ns
t _{dis}	$\overline{\text{OE}}$	Y	1.5	7		7.7	ns
t _{sk(o)} [§]				1			ns

[§] Skew between any two outputs of the same package switching in the same direction. This parameter is warranted but not production tested.

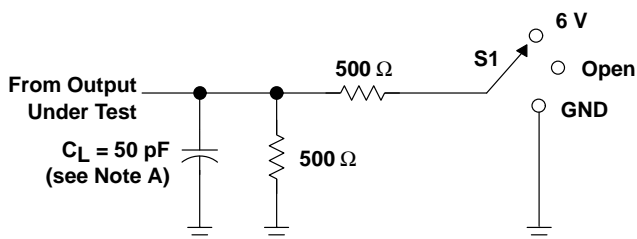
operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance per buffer/driver	C _L = 50 pF, f = 10 MHz	20.2	pF
	Outputs enabled Outputs disabled		3.6	



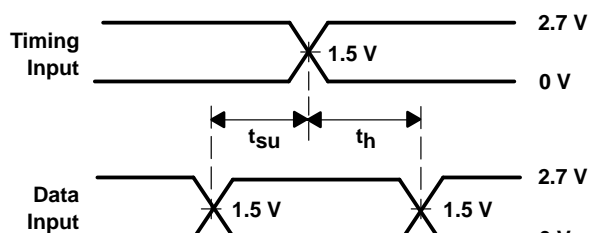
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PARAMETER MEASUREMENT INFORMATION

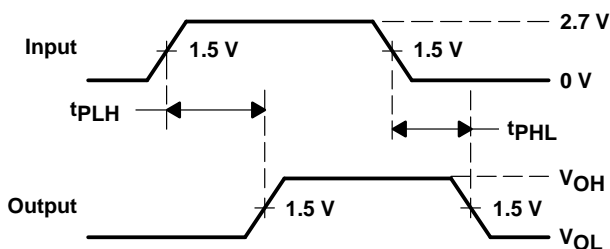


LOAD CIRCUIT

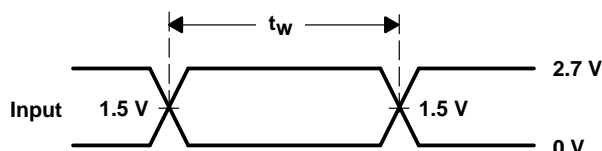
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



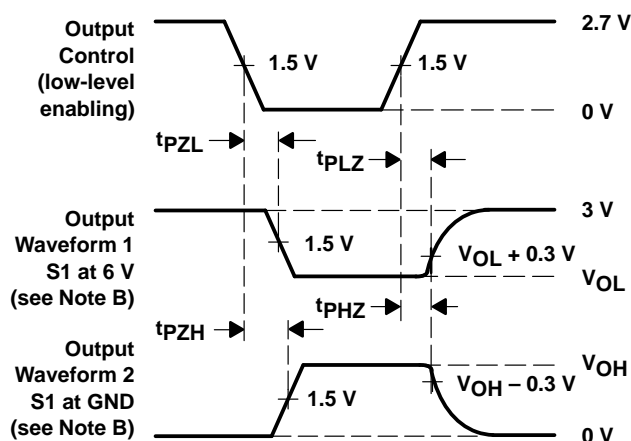
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

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