

SN74LVCH16245A

16-BIT BUS TRANSCEIVER

WITH 3-STATE OUTPUTS

SCES063A – DECEMBER 1995 – REVISED JUNE 1996

- Member of the Texas Instruments *Widebus™* Family
- *EPIC™* (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 16-bit (dual-octal) noninverting bus transceiver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVCH16245A is designed for asynchronous communication between data buses. The control-function implementation minimizes external timing requirements.

This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so that the buses are effectively isolated.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVCH16245A is characterized for operation from -40°C to 85°C .

DGG OR DL PACKAGE
(TOP VIEW)

| | | | |
|----------|----|----|------------------|
| 1DIR | 1 | 48 | $\overline{1OE}$ |
| 1B1 | 2 | 47 | 1A1 |
| 1B2 | 3 | 46 | 1A2 |
| GND | 4 | 45 | GND |
| 1B3 | 5 | 44 | 1A3 |
| 1B4 | 6 | 43 | 1A4 |
| V_{CC} | 7 | 42 | V_{CC} |
| 1B5 | 8 | 41 | 1A5 |
| 1B6 | 9 | 40 | 1A6 |
| GND | 10 | 39 | GND |
| 1B7 | 11 | 38 | 1A7 |
| 1B8 | 12 | 37 | 1A8 |
| 2B1 | 13 | 36 | 2A1 |
| 2B2 | 14 | 35 | 2A2 |
| GND | 15 | 34 | GND |
| 2B3 | 16 | 33 | 2A3 |
| 2B4 | 17 | 32 | 2A4 |
| V_{CC} | 18 | 31 | V_{CC} |
| 2B5 | 19 | 30 | 2A5 |
| 2B6 | 20 | 29 | 2A6 |
| GND | 21 | 28 | GND |
| 2B7 | 22 | 27 | 2A7 |
| 2B8 | 23 | 26 | 2A8 |
| 2DIR | 24 | 25 | $\overline{2OE}$ |



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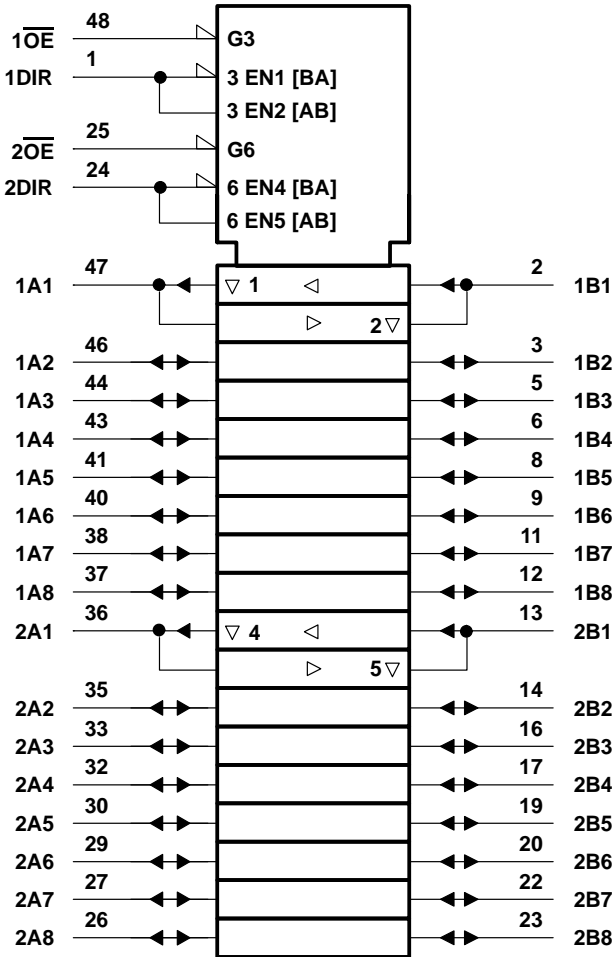
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FUNCTION TABLE

(each 8-bit section)

| INPUTS | | OPERATION |
|--------|-----|-----------------|
| OE | DIR | |
| L | L | B data to A bus |
| L | H | A data to B bus |
| H | X | Isolation |

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

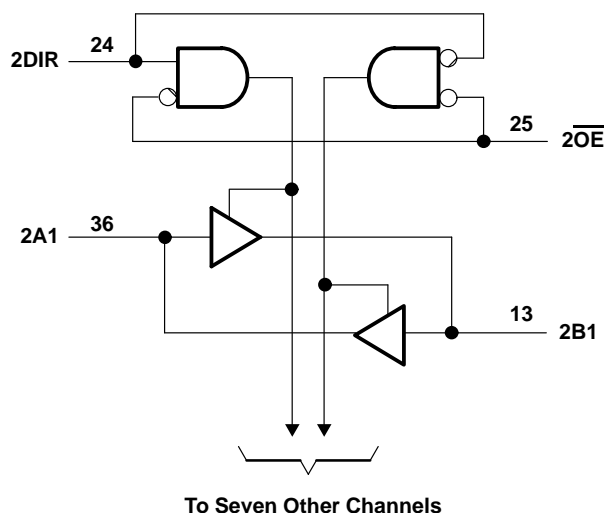
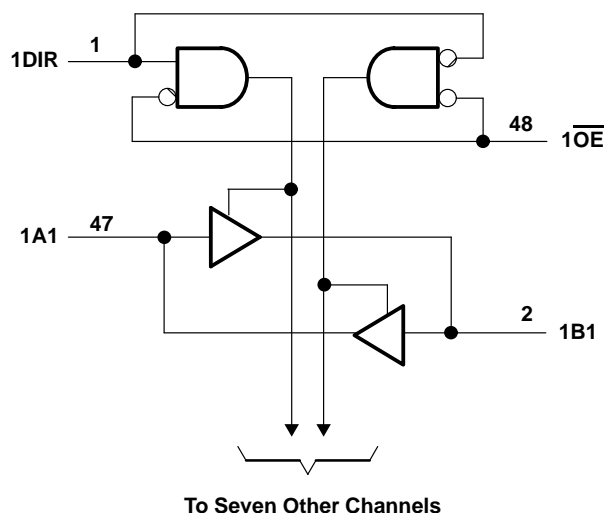
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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

| | |
|--|----------------------------|
| Supply voltage range, V_{CC} | –0.5 V to 6.5 V |
| Input voltage range, V_I : Except I/O ports (see Note 1) | –0.5 V to 6.5 V |
| I/O ports (see Notes 1 and 2) | –0.5 V to $V_{CC} + 0.5$ V |
| Voltage applied to any output in the high-impedance state or power-off state, V_O (see Note 1) | –0.5 V to 6.5 V |
| Voltage applied to any output in the high or low state, V_O (see Notes 1 and 2) | –0.5 V to $V_{CC} + 0.5$ V |
| Input clamp current, I_{IK} ($V_I < 0$) | –50 mA |
| Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) | ±50 mA |
| Continuous output current, I_O ($V_O = 0$ to V_{CC}) | ±50 mA |
| Continuous current through each V_{CC} or GND | ±100 mA |
| Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 3): DGG package | 0.85 W |
| DL package | 1.2 W |
| Storage temperature range, T_{stg} | –65°C to 150°C |

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This value is limited to 4.6 V maximum.
 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*.

recommended operating conditions (see Note 4)

| | | | MIN | MAX | UNIT |
|---------------------|------------------------------------|---|-----|----------|------|
| V_{CC} | Supply voltage | Operating | 2 | 3.6 | V |
| | | Data retention only | 1.5 | | |
| V_{IH} | High-level input voltage | $V_{CC} = 2.7\text{ V to }3.6\text{ V}$ | 2 | | V |
| V_{IL} | Low-level input voltage | $V_{CC} = 2.7\text{ V to }3.6\text{ V}$ | | 0.8 | V |
| V_I | Input voltage | | 0 | 5.5 | V |
| V_O | Output voltage | High or low state | 0 | V_{CC} | V |
| | | 3 state | 0 | 5.5 | |
| I_{OH} | High-level output current | $V_{CC} = 2.7\text{ V}$ | | -12 | mA |
| | | $V_{CC} = 3\text{ V}$ | | -24 | |
| I_{OL} | Low-level output current | $V_{CC} = 2.7\text{ V}$ | | 12 | mA |
| | | $V_{CC} = 3\text{ V}$ | | 24 | |
| $\Delta t/\Delta V$ | Input transition rise or fall rate | | 0 | 5 | ns/V |
| T_A | Operating free-air temperature | | -40 | 85 | °C |

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} [†] | MIN | TYP [‡] | MAX | UNIT |
|------------------------------|----------------|--|------------------------------|-----------------------|------------------|------|------|
| V _{OH} | | I _{OH} = −100 μA | MIN to MAX | V _{CC} − 0.2 | | | V |
| | | I _{OH} = −12 mA | 2.7 V | 2 | | | |
| | | | 3 V | 2.2 | | | |
| | | I _{OH} = −24 mA | 3 V | 2 | | | |
| V _{OL} | | I _{OL} = 100 μA | MIN to MAX | 0.2 | | | V |
| | | I _{OL} = 12 mA | 2.7 V | 0.4 | | | |
| | | I _{OL} = 24 mA | 3 V | 0.55 | | | |
| I _I | Control inputs | V _I = 5.5 V or GND | 3.6 V | | | ±5 | μA |
| I _I (hold) | | V _I = 0.8 V | 3 V | 75 | | | μA |
| | | V _I = 2 V | | −75 | | | |
| | | V _I = 0 to 3.6 V [§] | 3.6 V | | | ±500 | |
| I _{off} | | V _I or V _O = 5.5 V | 0 | | | 50 | μA |
| I _{OZ} [¶] | | V _O = 0 or 5.5 V | 3.6 V | | | ±20 | μA |
| I _{CC} | | V _I = V _{CC} or GND, I _O = 0 | 3.6 V | | | 20 | μA |
| ΔI _{CC} | | One input at V _{CC} − 0.6 V, Other inputs at V _{CC} or GND | 2.7 V to 3.6 V | | | 500 | μA |
| C _i | Control inputs | V _I = V _{CC} or GND | 3.3 V | 5.4 | | | pF |
| C _{io} | A or B ports | V _O = V _{CC} or GND | 3.3 V | 9 | | | pF |

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

‡ All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

§ This is the bus-hold maximum dynamic current required to switch the input from one state to another.

¶ For I/O ports, the parameter I_{OZ} includes the input leakage current, but not $I_{I(\text{hold})}$.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$ | | $V_{CC} = 2.7\text{ V}$ | | UNIT |
|---------------------|-----------------|----------------|---|-----|-------------------------|-----|------|
| | | | MIN | MAX | MIN | MAX | |
| t_{pd} | A or B | B or A | 1 | 5.2 | 5.8 | | ns |
| t_{en} | \overline{OE} | A or B | 1.5 | 7.2 | 8 | | ns |
| t_{dis} | \overline{OE} | A or B | 1.5 | 7.2 | 8 | | ns |
| $t_{sk(o)}^\dagger$ | | | | 1 | | | ns |

† Skew between any two outputs of the same package switching in the same direction. This parameter is warranted but not production tested.

operating characteristics, $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$

| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|-----------|---|------------------|---|-----|------|
| C_{pd} | Power dissipation capacitance per transceiver | Outputs enabled | $C_L = 50\text{ pF}$, $f = 10\text{ MHz}$ | 24 | pF |
| | | Outputs disabled | | 3.7 | |



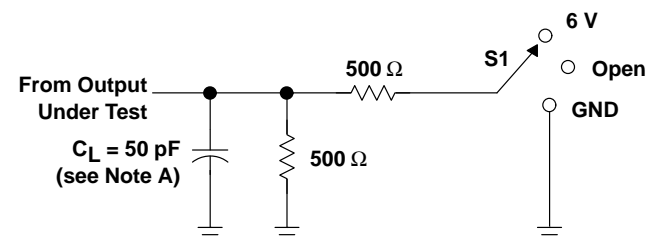
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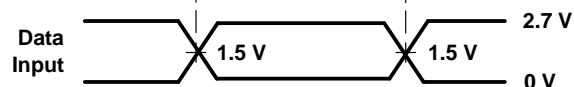
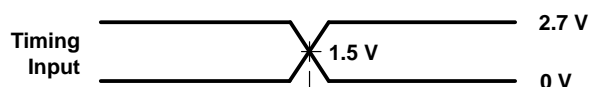
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PARAMETER MEASUREMENT INFORMATION

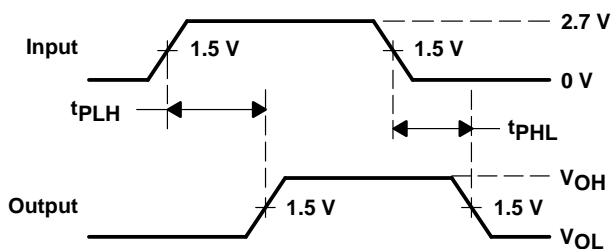


LOAD CIRCUIT

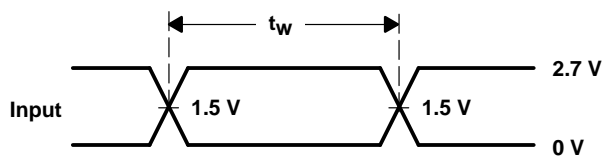
| TEST | S1 |
|-------------------|------|
| t_{pd} | Open |
| t_{PLZ}/t_{PZL} | 6 V |
| t_{PHZ}/t_{PZH} | GND |



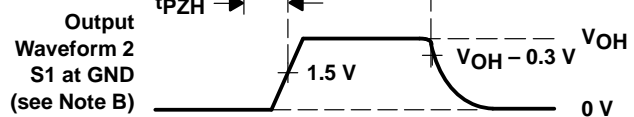
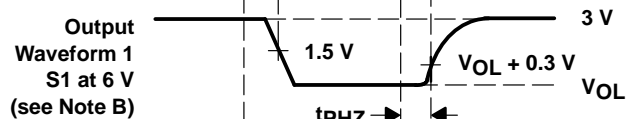
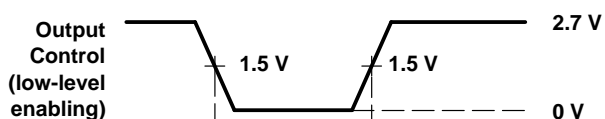
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

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