

- Member of the Texas Instruments *Widebus™* Family
- *EPIC™* (Enhanced-Performance Implanted CMOS) Submicron Process
- High-Impedance State During Power Up
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Plastic 300-mil Thin Shrink Small-Outline Package

description

This 1-bit-to-4-bit address register/driver is designed for 2.3-V to 3.6-V V_{CC} operation. The device is ideal for use in applications where a single address bus is driving four separate memory locations. The SN74ALVCH16831 can be used as a buffer or a register, depending on the logic level of the select (\overline{SEL}) input.

When \overline{SEL} is logic high, the device is in the buffer mode. The outputs follow the inputs and are controlled by the two output-enable (\overline{OE}) controls. Each \overline{OE} controls two groups of nine outputs.

When \overline{SEL} is logic low, the device is in the register mode. The register is an edge-triggered D-type flip-flop. On the positive transition of the clock (CLK) input, data set up at the A inputs is stored in the internal registers. \overline{OE} controls operate the same as in buffer mode.

When \overline{OE} is logic low, the outputs are in a normal logic state (high or low logic level). When \overline{OE} is logic high, the outputs are in the high-impedance state.

\overline{SEL} or \overline{OE} does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

When V_{CC} is between 0 and 1.2 V, the device is in the high-impedance state during power up. However, to ensure the high-impedance state above 1.2 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

DBB PACKAGE
(TOP VIEW)

4Y1	1	80	1Y2
3Y1	2	79	2Y2
GND	3	78	GND
2Y1	4	77	3Y2
1Y1	5	76	4Y2
V_{CC}	6	75	V_{CC}
NC	7	74	1Y3
A1	8	73	2Y3
GND	9	72	GND
NC	10	71	3Y3
A2	11	70	4Y3
GND	12	69	GND
NC	13	68	1Y4
A3	14	67	2Y4
V_{CC}	15	66	V_{CC}
NC	16	65	3Y4
A4	17	64	4Y4
GND	18	63	GND
CLK	19	62	1Y5
$\overline{OE1}$	20	61	2Y5
$\overline{OE2}$	21	60	3Y5
\overline{SEL}	22	59	4Y5
GND	23	58	GND
A5	24	57	1Y6
A6	25	56	2Y6
V_{CC}	26	55	V_{CC}
A7	27	54	3Y6
NC	28	53	4Y6
GND	29	52	GND
A8	30	51	1Y7
NC	31	50	2Y7
GND	32	49	GND
A9	33	48	3Y7
NC	34	47	4Y7
V_{CC}	35	46	V_{CC}
4Y9	36	45	1Y8
3Y9	37	44	2Y8
GND	38	43	GND
2Y9	39	42	3Y8
1Y9	40	41	4Y8

NC – No internal connection

PRODUCT PREVIEW



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SN74ALVCH16831
1-TO-4 ADDRESS REGISTER/DRIVER
WITH 3-STATE OUTPUTS

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description (continued)

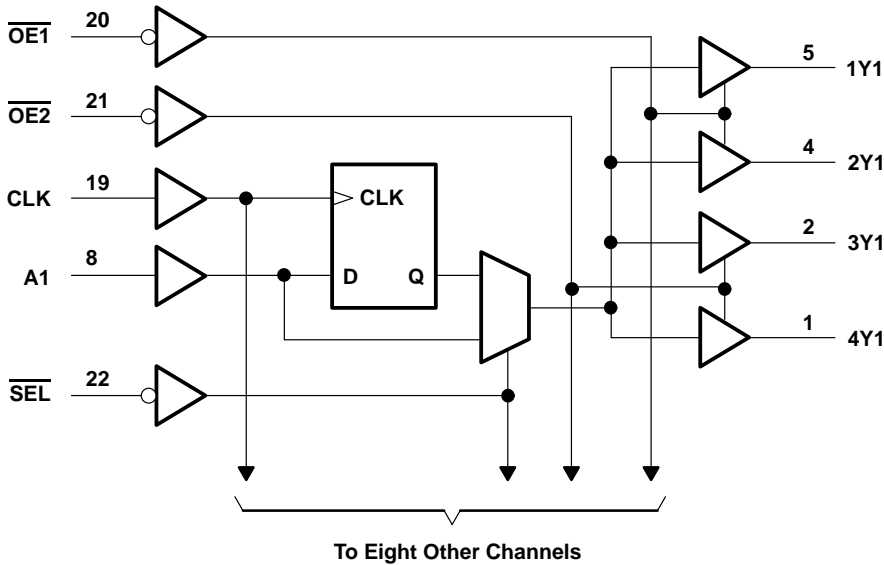
Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16831 is available in TI's thin-shrink small-outline (DBB) package, which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed circuit board area.

The SN74ALVCH16831 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE				
INPUTS				OUTPUT Y
\overline{OE}	\overline{SEL}	CLK	A	
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	↑	L	L
L	L	↑	H	H

logic diagram (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through each V_{CC} or GND	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 3)	0.84 W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This value is limited to 4.6 V maximum.
 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*.

recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.3	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.3$ V to 2.7 V	1.7	V
		$V_{CC} = 2.7$ V to 3.6 V	2	
V_{IL}	Low-level input voltage	$V_{CC} = 2.3$ V to 2.7 V	0.7	V
		$V_{CC} = 2.7$ V to 3.6 V	0.8	
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2.3$ V	–12	mA
		$V_{CC} = 2.7$ V	–12	
		$V_{CC} = 3$ V	–24	
I_{OL}	Low-level output current	$V_{CC} = 2.3$ V	12	mA
		$V_{CC} = 2.7$ V	12	
		$V_{CC} = 3$ V	24	
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		μs/V
T_A	Operating free-air temperature	–40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

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WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP†	MAX	UNIT
V _{OH}	I _{OH} = –100 µA	3 V to 3.6 V	V _{CC} – 0.2			V
	I _{OH} = –6 mA, V _{IH} = 1.7 V	2.3 V	2			
	I _{OH} = –12 mA	V _{IH} = 1.7 V	2.3 V		1.7	
		V _{IH} = 2 V	2.7 V		2.2	
			3 V		2.4	
	I _{OH} = –24 mA, V _{IH} = 2 V	3 V	2			
V _{OL}	I _{OL} = 100 µA	3 V to 3.6 V			0.2	V
	I _{OL} = 6 mA, V _{IL} = 0.7 V	2.3 V			0.4	
	I _{OL} = 12 mA	V _{IL} = 0.7 V	2.3 V		0.7	
		V _{IL} = 0.8 V	2.7 V		0.4	
	I _{OL} = 24 mA, V _{IL} = 0.8 V	3 V			0.55	
I _I	V _I = V _{CC} or GND	3.6 V			±5	µA
I _{I(hold)}	V _I = 0.7 V	2.3 V	45			µA
	V _I = 1.7 V		–45			
	V _I = 0.8 V	3 V	75			
	V _I = 2 V		–75			
	V _I = 0 to 3.6 V‡	3.6 V			±500	
I _{OZ}	V _O = V _{CC} or GND	3.6 V			±10	µA
I _{OZPU} §	V _O = 0.5 V to V _{CC} , $\overline{\text{OE}}$ = don't care	0 to 1.2 V			±10	µA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V			40	µA
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	3 V to 3.6 V			750	µA
C _i	Control inputs	3.3 V				pF
	Data inputs					
C _o	Outputs	3.3 V				pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

‡ This is the bus-hold maximum dynamic current required to switch the input from one state to another.

§ This parameter is specified by characterization.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency	0	150	0	150	0	150	MHz
t _w	Pulse duration, CLK high or low							ns
t _{su}	Setup time, A data before CLK↑							ns
t _h	Hold time, A data after CLK↑							ns



switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			150		150		150		MHz
t_{pd}	A	Y							ns
	CLK								
	$\overline{\text{SEL}}$								
t_{en}	$\overline{\text{OE}}$	Y							ns
t_{dis}	$\overline{\text{OE}}$	Y							ns

operating characteristics, $T_A = 25^\circ\text{C}$

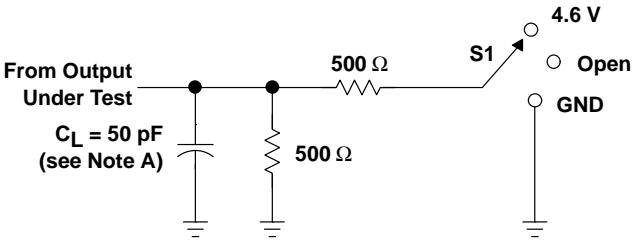
PARAMETER			TEST CONDITIONS	$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	UNIT
				TYP	TYP	
C_{pd} Power dissipation capacitance	Outputs enabled	$C_L = 0\text{ pF}, f = 10\text{ MHz}$				pF
	Outputs disabled					

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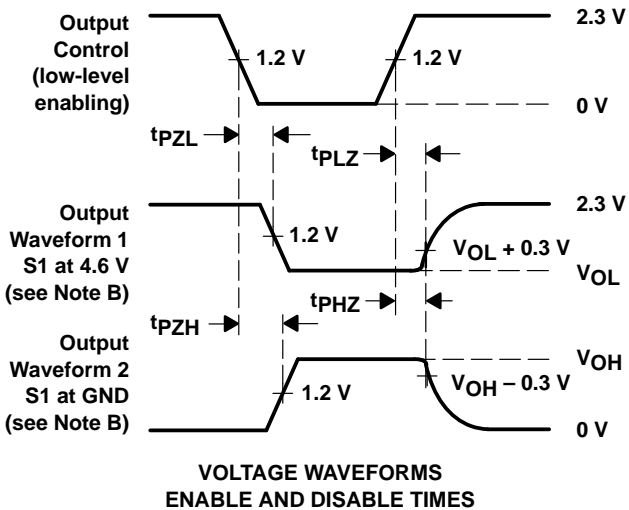
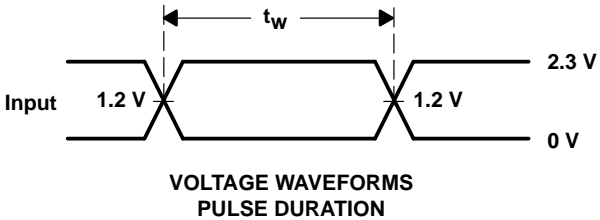
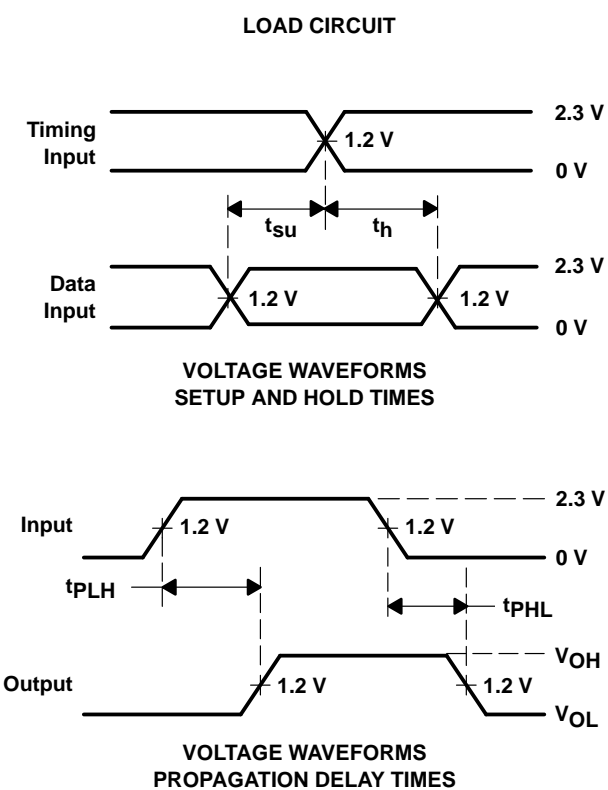
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PARAMETER MEASUREMENT INFORMATION
 $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$



TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	4.6 V
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT

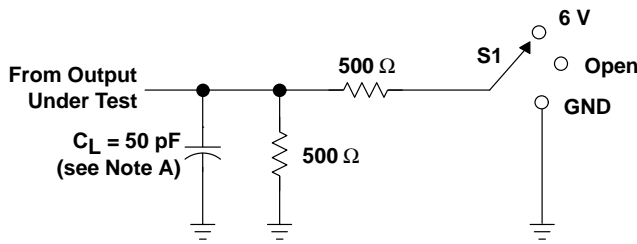


- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PHL} and t_{PLH} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

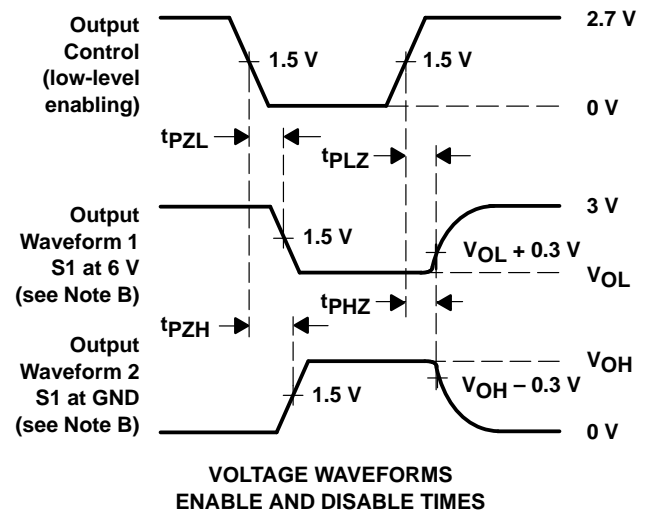
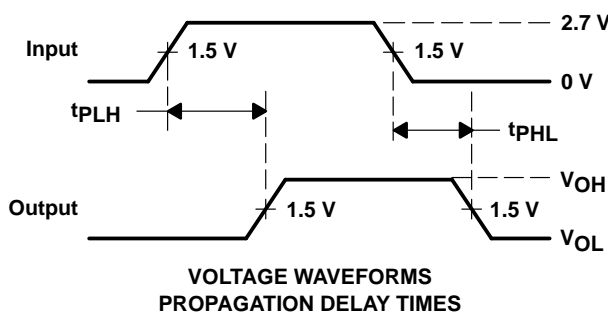
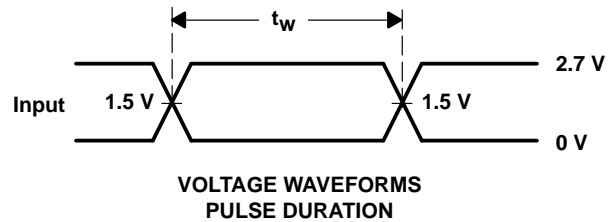
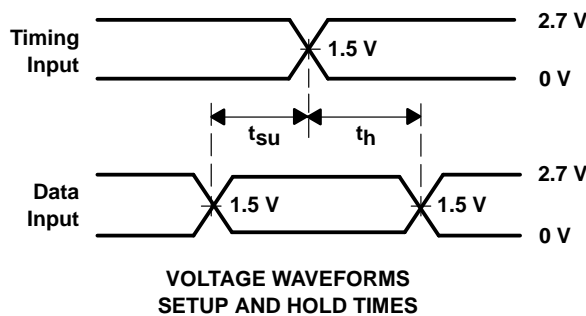
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PHL} and t_{PLH} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

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