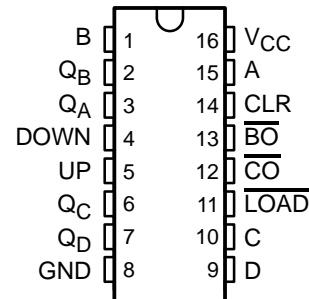


# SN54HC193, SN74HC193 4-BIT SYNCHRONOUS UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

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- Look-Ahead Circuitry Enhances Cascaded Counters
- Fully Synchronous in Count Modes
- Parallel Asynchronous Load for Modulo-N Count Lengths
- Asynchronous Clear
- Package Options Include Plastic Small-Outline (D) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

SN54HC193 . . . J OR W PACKAGE  
SN74HC193 . . . D OR N PACKAGE  
(TOP VIEW)



## description

The 'HC193 are 4-bit synchronous, reversible, up/down binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidentally with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple-clock) counters.

The outputs of the four flip-flops are triggered on a low-to-high-level transition of either count (clock) input (UP or DOWN). The direction of counting is determined by which count input is pulsed while the other count input is high.

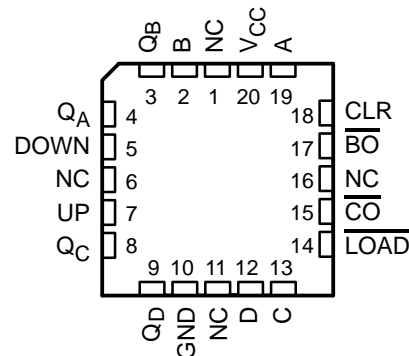
All four counters are fully programmable; that is, each output may be preset to either level by placing a low on the load ( $\overline{LOAD}$ ) input and entering the desired data at the data inputs. The output changes to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A clear (CLR) input has been provided that forces all outputs to the low level when a high level is applied. The clear function is independent of the count and  $\overline{LOAD}$  inputs.

These counters were designed to be cascaded without the need for external circuitry. The borrow ( $\overline{BO}$ ) output produces a low-level pulse while the count is zero (all outputs low) and DOWN is low. Similarly, the carry ( $\overline{CO}$ ) output produces a low-level pulse while the count is maximum (9 or 15) and UP is low. The counters can then be easily cascaded by feeding  $\overline{BO}$  and  $\overline{CO}$  to DOWN and UP, respectively, of the succeeding counter.

The SN54HC193 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74HC193 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

SN54HC193 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

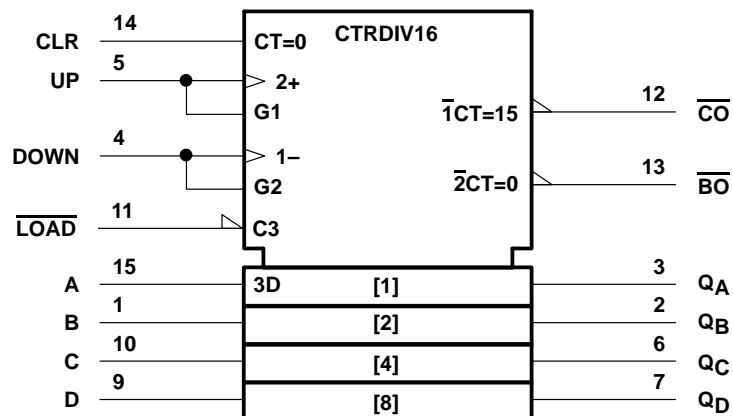
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# SN54HC193, SN74HC193 4-BIT SYNCHRONOUS UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

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## logic symbol†

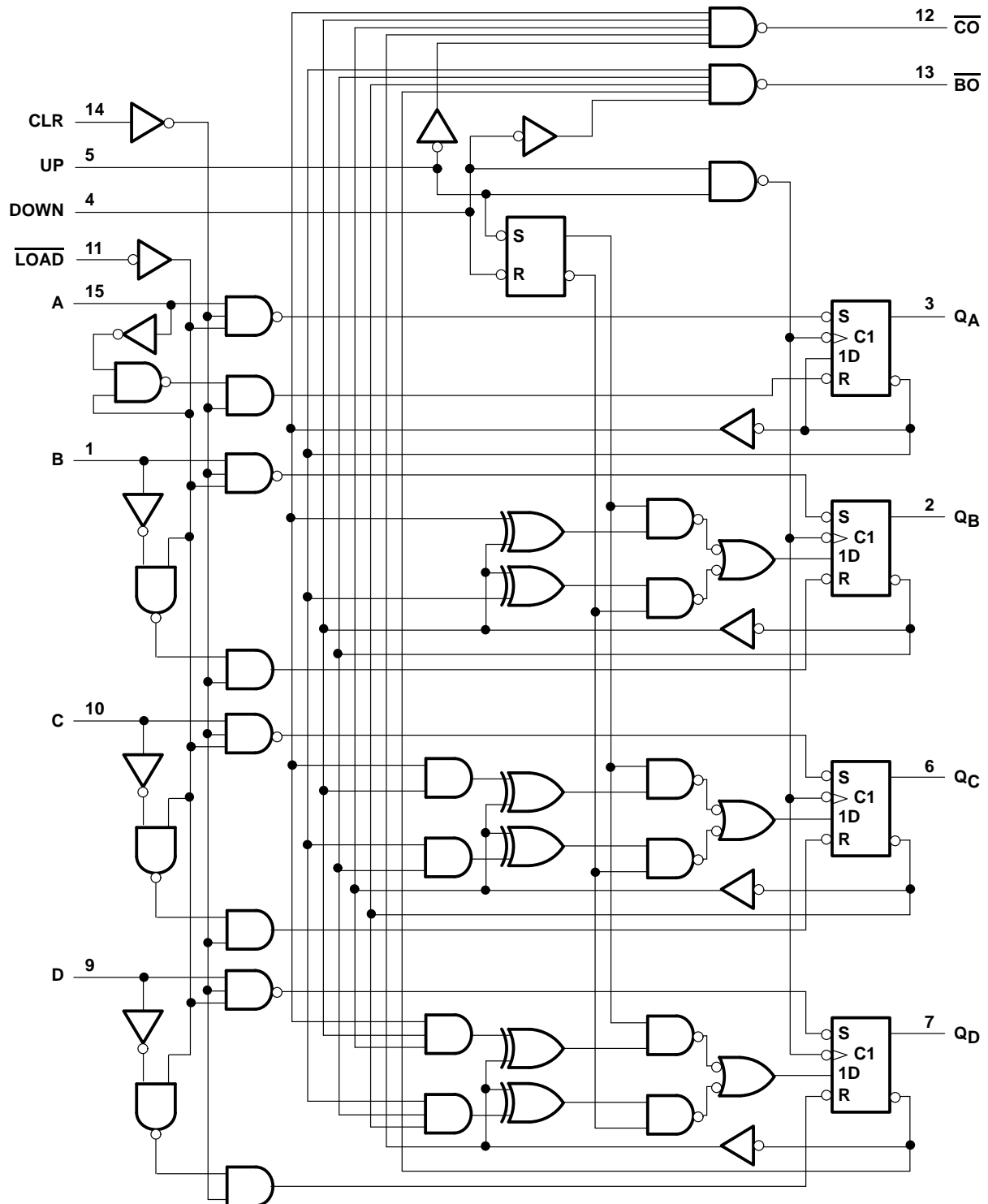


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.  
Pin numbers shown are for the D, J, N, and W packages.

**SN54HC193, SN74HC193**  
**4-BIT SYNCHRONOUS UP/DOWN COUNTERS**  
**(DUAL CLOCK WITH CLEAR)**

SCLS122A – DECEMBER 1982 – REVISED JANUARY 1996

logic diagram (positive logic)



Pin numbers shown are for the D, J, N, and W packages.

# SN54HC193, SN74HC193

## 4-BIT SYNCHRONOUS UP/DOWN COUNTERS

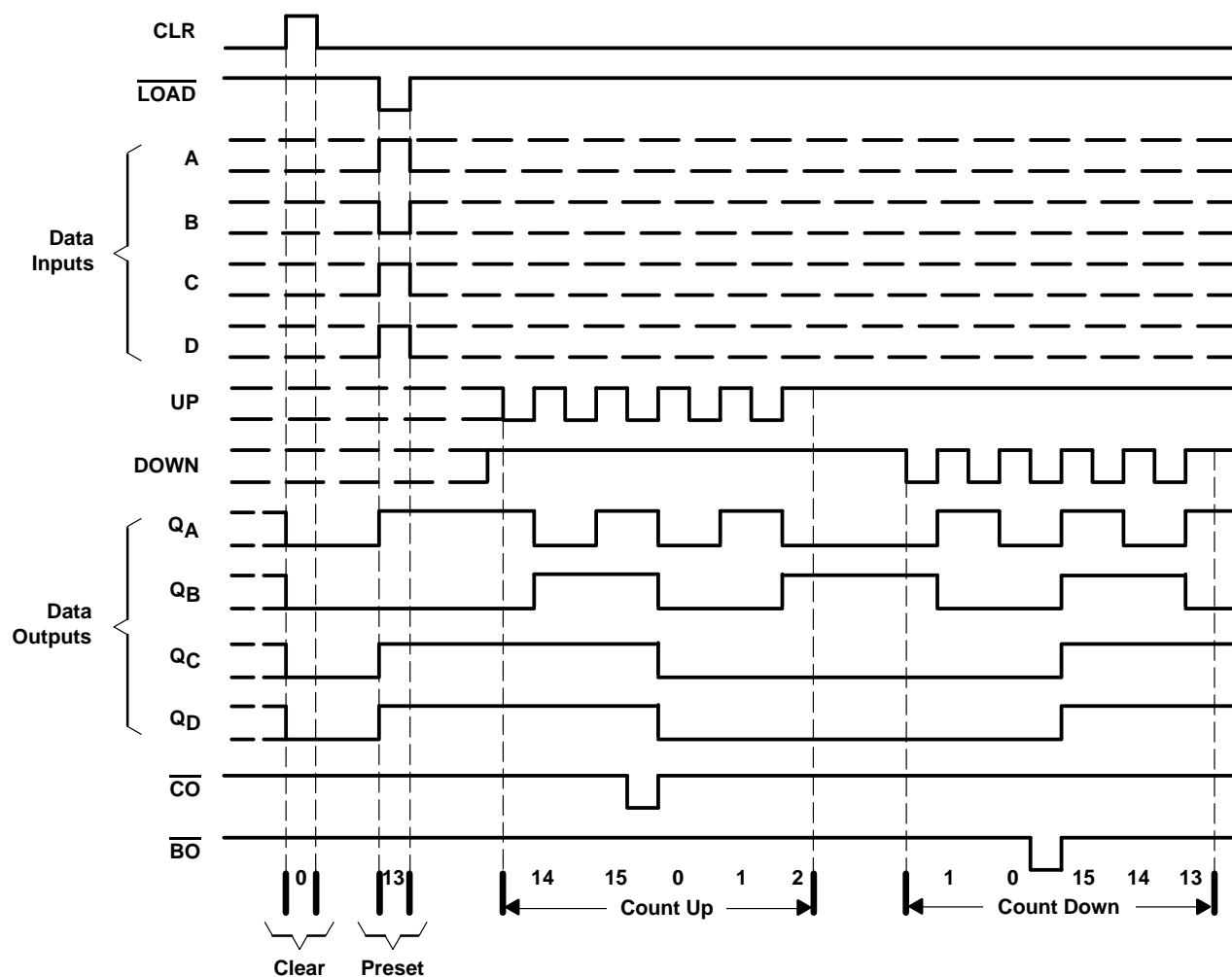
### (DUAL CLOCK WITH CLEAR)

SCLS122A – DECEMBER 1982 – REVISED JANUARY 1996

#### typical clear, load, and count sequence

The following sequence is illustrated below:

1. Clear outputs to 0
2. Load (preset) to binary 13
3. Count up to 14, 15, carry, 0, 1, and 2
4. Count down to 1, 0, borrow, 15, 14, and 13



NOTES: A. CLR overrides  $\overline{\text{LOAD}}$ , data, and count inputs.

B. When counting up, count-down input must be high; when counting down, count-up input must be high.

# SN54HC193, SN74HC193

## 4-BIT SYNCHRONOUS UP/DOWN COUNTERS

### (DUAL CLOCK WITH CLEAR)

SCLS122A – DECEMBER 1982 – REVISED JANUARY 1996

#### absolute maximum ratings over operating free-air temperature†

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) (see Note 1)	±20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) (see Note 1)	±20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±25 mA
Continuous current through $V_{CC}$ or GND	±50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2): D package	1.3 W
N package	1.1 W
Storage temperature range, $T_{stg}$	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

#### recommended operating conditions

			SN54HC193			SN74HC193			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage		2	5	6	2	5	6	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2 V	1.5			1.5			V
		V <sub>CC</sub> = 4.5 V	3.15			3.15			
		V <sub>CC</sub> = 6 V	4.2			4.2			
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2 V	0			0			V
		V <sub>CC</sub> = 4.5 V	0			1.35			
		V <sub>CC</sub> = 6 V	0			1.8			
V <sub>I</sub>	Input voltage		0		V <sub>CC</sub>	0		V <sub>CC</sub>	V
V <sub>O</sub>	Output voltage		0		V <sub>CC</sub>	0		V <sub>CC</sub>	V
t <sub>t</sub> <sup>†</sup>	Input transition (rise and fall) time	V <sub>CC</sub> = 2 V	0		1000	0		1000	ns
		V <sub>CC</sub> = 4.5 V	0		500	0		500	
		V <sub>CC</sub> = 6 V	0		400	0		400	
T <sub>A</sub>	Operating free-air temperature		−55		125	−40		85	°C

‡ If this device is used in the threshold region (from  $V_{IL\text{max}} = 0.5\text{ V}$  to  $V_{IH\text{min}} = 1.5\text{ V}$ ), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at  $t_t = 1000\text{ ns}$  and  $V_{CC} = 2\text{ V}$  will not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.



**SN54HC193, SN74HC193**  
**4-BIT SYNCHRONOUS UP/DOWN COUNTERS**  
**(DUAL CLOCK WITH CLEAR)**

SCLS122A – DECEMBER 1982 – REVISED JANUARY 1996

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS		V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HC193		SN74HC193		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -20 µA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I <sub>OH</sub> = -4 mA	4.5 V	3.98	4.3		3.7		3.84		
		I <sub>OH</sub> = -5.2 mA	6 V	5.48	5.8		5.2		5.34		
V <sub>OL</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 20 µA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I <sub>OL</sub> = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I <sub>OL</sub> = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0		6 V		±0.1	±100		±1000		±1000	nA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0, I <sub>O</sub> = 0		6 V			8		160		80	µA
C <sub>i</sub>			2 V to 6 V		3	10		10		10	pF

**timing requirements over recommended operating free-air temperature range (unless otherwise noted)**

		V <sub>CC</sub>	T <sub>A</sub> = 25°C		SN54HC193		SN74HC193		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency	2 V	0	4.2	0	2.8	0	3.3	MHz
		4.5 V	0	21	0	14	0	17	
		6 V	0	24	0	16	0	19	
t <sub>w</sub>	CLR high	2 V	120		180		150		ns
		4.5 V	24		36		30		
		6 V	21		31		26		
	$\overline{\text{LOAD}}$ low	2 V	120		180		150		
		4.5 V	24		36		30		
		6 V	21		31		26		
	UP or DOWN high or low	2 V	120		180		150		
		4.5 V	24		36		30		
		6 V	21		31		26		
t <sub>su</sub>	Data before $\overline{\text{LOAD}}$ inactive	2 V	110		165		140		ns
		4.5 V	22		33		28		
		6 V	19		28		24		
	CLR inactive before UP↑ or DOWN↑	2 V	110		165		140		
		4.5 V	22		33		28		
		6 V	19		28		24		
	$\overline{\text{LOAD}}$ inactive before UP↑ or DOWN↑	2 V	110		165		140		
		4.5 V	22		33		28		
		6 V	19		28		24		
t <sub>h</sub>	Data after $\overline{\text{LOAD}}$ inactive	2 V	5		5		5		ns
		4.5 V	5		5		5		
		6 V	5		5		5		



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**SN54HC193, SN74HC193**  
**4-BIT SYNCHRONOUS UP/DOWN COUNTERS**  
**(DUAL CLOCK WITH CLEAR)**

SCLS122A – DECEMBER 1982 – REVISED JANUARY 1996

switching characteristics over recommended operating free-air temperature range,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	$T_A = 25^\circ\text{C}$			SN54HC193		SN74HC193		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{\max}$			2 V	4.2	8		2.8		3.3		MHz
			4.5 V	21	55		14		17		
			6 V	24	60		16		19		
$t_{pd}$	UP	$\overline{CO}$	2 V		75	165		250		205	ns
			4.5 V		24	33		50		41	
			6 V		20	28		43		35	
	DOWN	$\overline{BO}$	2 V		75	165		250		205	
			4.5 V		24	33		50		41	
			6 V		20	28		43		35	
	UP or DOWN	Any Q	2 V		190	250		375		315	
			4.5 V		40	50		75		63	
			6 V		35	43		64		54	
	$\overline{LOAD}$	Any Q	2 V		190	260		390		325	
			4.5 V		40	52		78		65	
			6 V		35	44		66		55	
$t_{PHL}$	CLR	Any Q	2 V		170	240		360		300	ns
			4.5 V		36	48		72		60	
			6 V		31	41		61		51	
$t_t$		Any	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

operating characteristics,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance	No load	50	pF

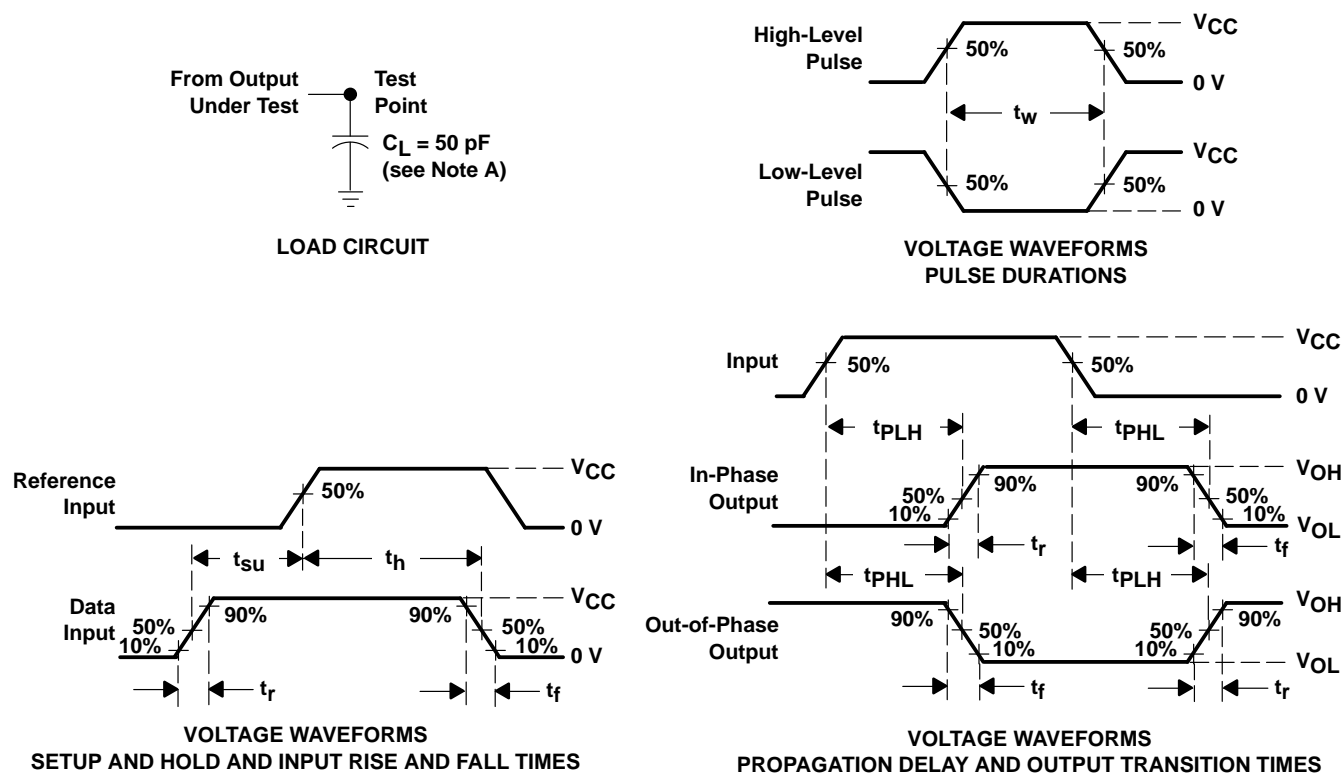
# SN54HC193, SN74HC193

## 4-BIT SYNCHRONOUS UP/DOWN COUNTERS

### (DUAL CLOCK WITH CLEAR)

SCLS122A – DECEMBER 1982 – REVISED JANUARY 1996

#### PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A.  $C_L$  includes probe and test-fixture capacitance.
  - B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = 6 \text{ ns}$ ,  $t_f = 6 \text{ ns}$ .
  - C. For clock inputs,  $f_{max}$  is measured when the input duty cycle is 50%.
  - D. The outputs are measured one at a time with one input transition per measurement.
  - E.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms



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