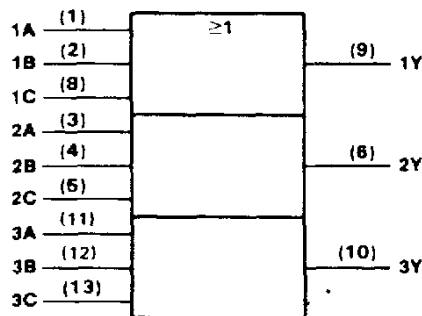


- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

**description**

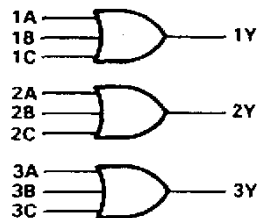
These devices contain three independent 3-input OR gates and perform the Boolean functions  $Y = A + B + C$  or  $Y = \bar{A} \cdot \bar{B} \cdot \bar{C}$  in positive logic.

The SN54HC4075 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74HC4075 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

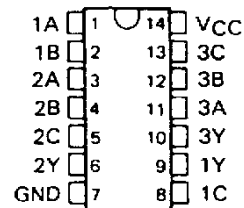
**logic symbol†**

†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

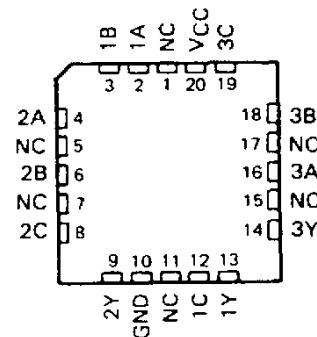
Pin numbers shown are for D, J, and N packages.

**logic diagram (positive logic)**

SN54HC4075 . . . J PACKAGE  
SN74HC4075 . . . D OR N PACKAGE  
(TOP VIEW)



SN54HC4075 . . . FK PACKAGE  
(TOP VIEW)



NC—No internal connection

**FUNCTION TABLE**

INPUTS			OUTPUT
A	B	C	Y
H	X	X	H
X	H	X	H
X	X	H	H
L	L	L	L

**. 54HC4075, SN74HC4075**  
**TRIPLE 3-INPUT OR GATES**

**absolute maximum ratings over operating free-air temperature range†**

Supply voltage, $V_{CC}$	-0.5 V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ )	$\pm 20$ mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	$\pm 20$ mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	$\pm 25$ mA
Continuous current through $V_{CC}$ or GND pins	$\pm 50$ mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package	300 °C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package	260 °C
Storage temperature range	-65 °C to 150 °C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**recommended operating conditions**

		SN54HC4075			SN74HC4075			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	2	5	6	2	5	6	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2$ V 1.5 $V_{CC} = 4.5$ V 3.15 $V_{CC} = 6$ V 4.2			1.5 3.15 4.2			V
$V_{IL}$	Low-level input voltage	$V_{CC} = 2$ V 0 $V_{CC} = 4.5$ V 0 $V_{CC} = 6$ V 0			0 0 0			V
$V_I$	Input voltage	0		$V_{CC}$	0		$V_{CC}$	V
$V_O$	Output voltage	0		$V_{CC}$	0		$V_{CC}$	V
$t_t$	Input transition (rise and fall) times	$V_{CC} = 2$ V 0 $V_{CC} = 4.5$ V 0 $V_{CC} = 6$ V 0			1000 500 400			ns
$T_A$	Operating free-air temperature	-55		125	-40		85	°C

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	$V_{CC}$	$T_A = 25^\circ\text{C}$			SN54HC4075		SN74HC4075		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$V_{OH}$	$V_I = V_{IH}$ or $V_{IL}$ , $I_{OH} = -20 \mu\text{A}$	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	$V_I = V_{IH}$ or $V_{IL}$ , $I_{OH} = -4 \text{ mA}$	4.5 V	3.98	4.30		3.7		3.84		
$V_{OL}$	$V_I = V_{IH}$ or $V_{IL}$ , $I_{OL} = 20 \mu\text{A}$	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	$V_I = V_{IH}$ or $V_{IL}$ , $I_{OL} = 4 \text{ mA}$	4.5 V		0.17	0.26		0.4		0.33	
	$V_I = V_{IH}$ or $V_{IL}$ , $I_{OL} = 5.2 \text{ mA}$	6 V		0.15	0.26		0.4		0.33	
$I_I$	$V_I = V_{CC}$ or 0	6 V	$\pm 0.1$		$\pm 100$	$\pm 1000$		$\pm 1000$		nA
$I_{CC}$	$V_I = V_{CC}$ or 0, $I_O = 0$	6 V			8	160		80		$\mu\text{A}$
$C_i$		2 to 6 V	3		10	10		10		pF



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**SN54HC4075, SN74HC4075**  
**TRIPLE 3-INPUT OR GATES**

switching characteristics over recommended operating free-air temperature range (unless otherwise noted),  $C_L = 50 \text{ pF}$  (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	$T_A = 25^\circ\text{C}$			SN54HC4075		SN74HC4075		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{pd}$	A, B, or C	Y	2 V		38	100		150		125	ns
			4.5 V		11	20		30		25	
			6 V		9	17		25		21	
$t_t$		Y	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

$C_{pd}$	Power dissipation capacitance per gate	No load, $T_A = 25^\circ\text{C}$	26 pF typ
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Note 1: Load circuits and voltage waveforms are shown in Section 1.



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