

SN54HCT652, SN74HCT652 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SCLS179A – MARCH 1984 – REVISED JANUARY 1996

- Inputs Are TTL-Voltage Compatible
- Independent Registers and Enables for A and B Buses
- Multiplexed Real-Time and Stored Data
- True Data Paths
- High-Current 3-State Outputs Can Drive up to 15 LSTTL Loads
- Package Options Include Plastic Small-Outline (DW) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (NT) and Ceramic (JT) 300-mil DIPs

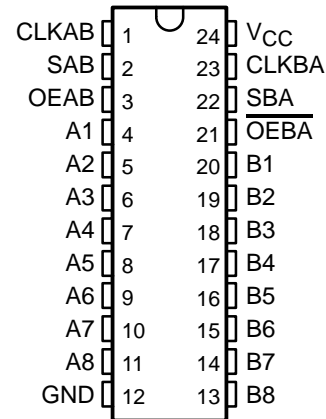
description

The 'HCT652 consist of bus-transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Output-enable (OEAB and $\overline{\text{OEBA}}$) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select real-time or stored data transfer. A low input level selects real-time data; a high input level selects stored data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'HCT652.

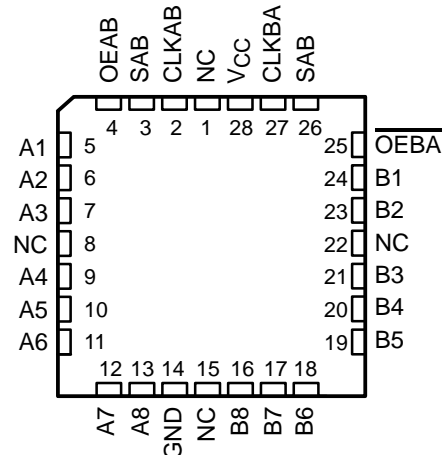
Data on the A or B data bus, or both, can be stored in the internal D-type flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) terminals regardless of the select- or output-control terminals. When SAB and SBA are in the real-time transfer mode, it is possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and $\overline{\text{OEBA}}$. In this configuration, each output reinforces its input. When all other data sources to the two sets of bus lines are at high impedance, each set of bus lines remains at its last state.

The SN54HCT652 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74HCT652 is characterized for operation from -40°C to 85°C .

SN54HCT652 . . . JT OR W PACKAGE
SN74HCT652 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54HCT652 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

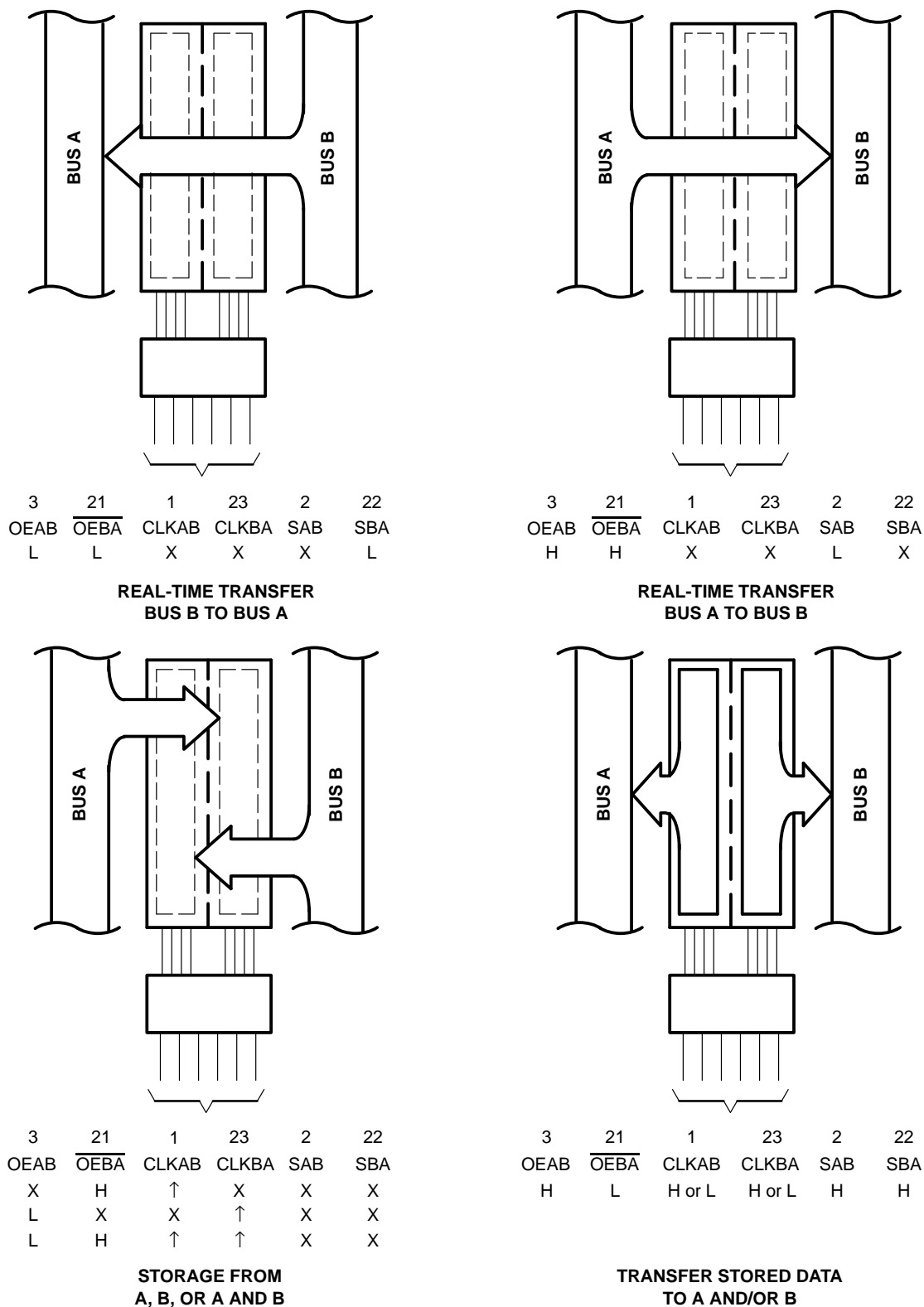
Copyright © 1996, Texas Instruments Incorporated

SN54HCT652, SN74HCT652

OCTAL BUS TRANSCEIVERS AND REGISTERS

WITH 3-STATE OUTPUTS

SCLS179A – MARCH 1984 – REVISED JANUARY 1996



Pin numbers are for the DW, JT, NT, and W packages.

Figure 1. Bus-Management Functions

SN54HCT652, SN74HCT652 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SCLS179A – MARCH 1984 – REVISED JANUARY 1996

FUNCTION TABLE

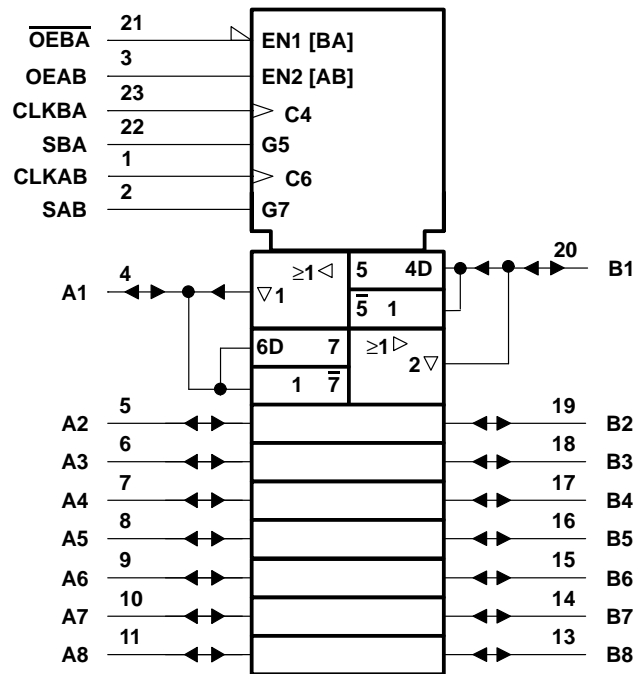
INPUTS						DATA I/O†		OPERATION OR FUNCTION
OEAB	OEBA	CLKAB	CLKBA	SAB	SBA	A1–A8	B1–B8	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B data
X	H	↑	H or L	X	X	Input	Unspecified‡	Store A, hold B
H	H	↑	↑	X‡	X	Input	Output	Store A in both registers
L	X	H or L	↑	X	X	Unspecified‡	Input	Hold A, store B
L	L	↑	↑	X	X‡	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
H	H	X	X	L	X	Input	Output	Real-time A data to B bus
H	H	H or L	X	H	X	Input	Output	Stored A data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored A data to B bus and stored B data to A bus

† The data-output functions can be enabled or disabled by a variety of level combinations at OEAB or OEBA. Data-input functions are always enabled; i.e., data at the bus terminals is stored on every low-to-high transition on the clock inputs.

‡ Select control = L; clocks can occur simultaneously.

Select control = H; clocks must be staggered to load both registers.

logic symbols§

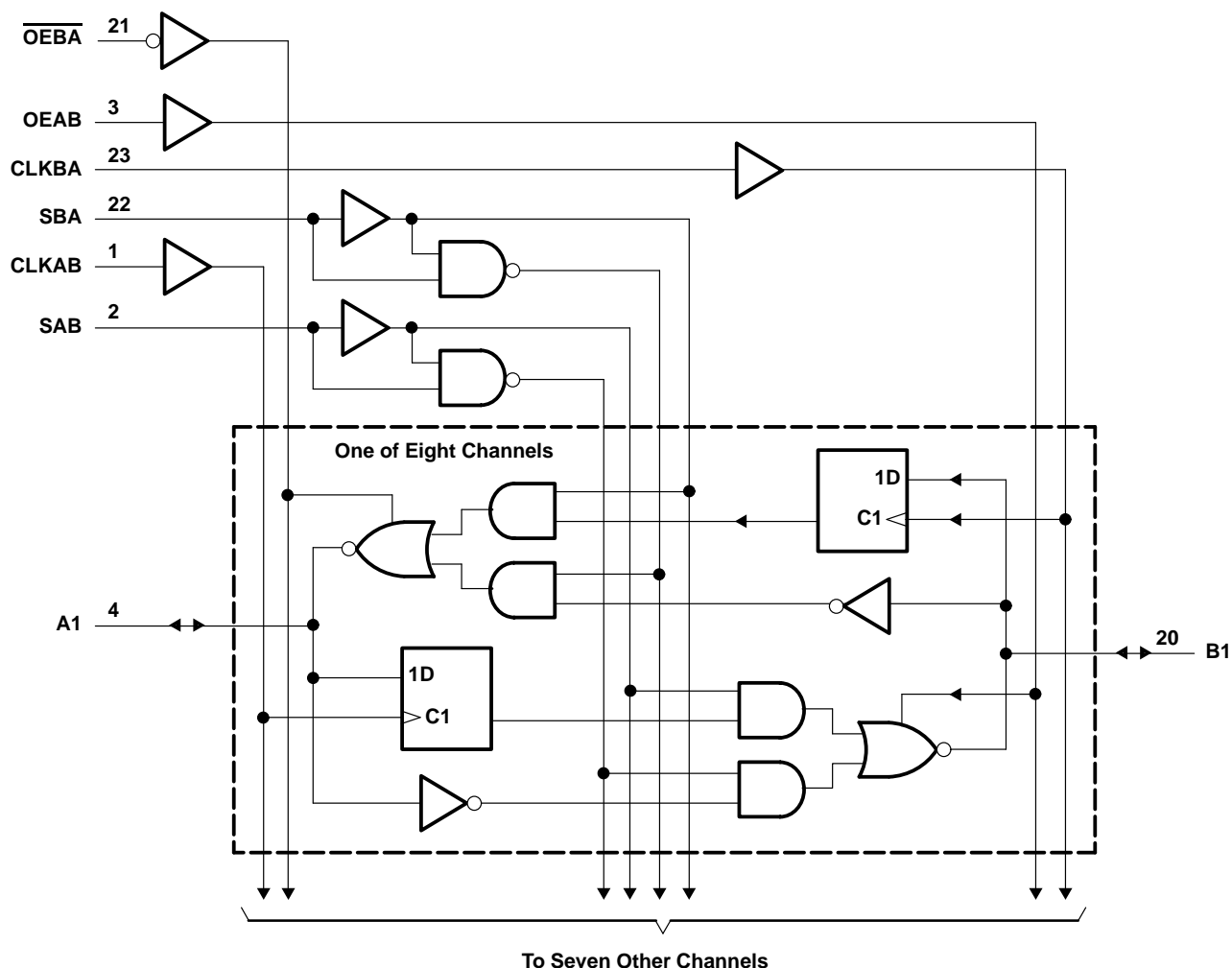


§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers are for the DW, JT, NT, and W packages.

SN54HCT652, SN74HCT652 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SCLS179A – MARCH 1984 – REVISED JANUARY 1996

logic diagram (positive logic)



Pin numbers are for the DW, JT, NT, and W packages.

absolute maximum ratings over operating free-air temperature†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1)	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±35 mA
Continuous current through V_{CC} or GND	±70 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2):	
DW package	1.7 W
NT package	1.3 W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the NT package, which has a trace length of zero.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN54HCT652, SN74HCT652 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SCLS179A – MARCH 1984 – REVISED JANUARY 1996

recommended operating conditions

			SN54HCT652			SN74HCT652			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 4.5 V to 5.5 V	2			2			V
V _{IL}	Low-level input voltage	V _{CC} = 4.5 V to 5.5 V	0		0.8	0		0.8	V
V _I	Input voltage		0		V _{CC}	0		V _{CC}	V
V _O	Output voltage		0		V _{CC}	0		V _{CC}	V
t _t	Input transition (rise and fall) time		0		500	0		500	ns
T _A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54HCT652		SN74HCT652		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}		V _I = V _{IH} or V _{IL} I _{OH} = –20 µA	4.5 V	4.4	4.499		4.4		4.4		V
				3.98	4.3		3.7		3.84		
V _{OL}		V _I = V _{IH} or V _{IL} I _{OL} = 20 µA	4.5 V		0.001	0.1		0.1		0.1	V
					0.17	0.26		0.4		0.33	
I _I	Control inputs	V _I = V _{CC} or 0	5.5 V	±0.1	±100		±1000		±1000		nA
I _{OZ}	A or B	V _O = V _{CC} or 0, V _I = V _{IH} or V _{IL} , Data = V _{CC} or 0	5.5 V	±0.01	±0.5		±10		±5		µA
I _{CC}		V _I = V _{CC} or 0, I _O = 0	5.5 V			8		160		80	µA
ΔI _{CC} †		One input at 0.5 V or 2.4 V, Other inputs at 0 or V _{CC}	5.5 V		1.4	2.4		3		2.9	mA
C _i	Control inputs		4.5 V to 5.5 V		3	10		10		10	pF

† This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 or V_{CC}.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V _{CC}	T _A = 25°C		SN54HCT652		SN74HCT652		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency	4.5 V	0	25	0	17	0	20	MHz
		5.5 V	0	28	0	19	0	22	
t _w	Pulse duration, CLKBA or CLKAB high or low	4.5 V	20		30		25		ns
		5.5 V	18		27		23		
t _{su}	Setup time, A before CLKAB↑ or B before CLKBA↑	4.5 V	15		23		19		ns
		5.5 V	14		21		17		
t _h	Hold time, A after CLKAB↑ or B after CLKBA↑	4.5 V	5		5		5		ns
		5.5 V	5		5		5		

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN54HCT652, SN74HCT652

OCTAL BUS TRANSCEIVERS AND REGISTERS

WITH 3-STATE OUTPUTS

SCLS179A – MARCH 1984 – REVISED JANUARY 1996

switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			SN54HCT652		SN74HCT652		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{\max}			4.5 V	25	35		17		20		MHz
			5.5 V	28	40		19		22		
t_{pd}	CLKBA or CLKAB	A or B	4.5 V		18	36		54		45	ns
			5.5 V		16	32		49		41	
	A or B	B or A	4.5 V		14	27		41		34	
			5.5 V		12	24		37		31	
	SBA or SAB†	A or B	4.5 V		20	38		57		48	
			5.5 V		17	34		51		43	
t_{en}	\overline{OEBA} or OEAB	A or B	4.5 V		25	49		74		61	ns
			5.5 V		22	44		67		55	
t_{dis}	\overline{OEBA} or OEAB	A or B	4.5 V		25	49		74		61	ns
			5.5 V		22	44		67		55	
t_t		Any	4.5 V		9	12		18		15	ns
			5.5 V		7	11		16		14	

† These parameters are measured with the internal output state of the storage register opposite that of the bus input.

switching characteristics over recommended operating free-air temperature range, $C_L = 150$ pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			SN54HCT652		SN74HCT652		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	CLKBA or CLKAB	A or B	4.5 V		24	53		80		66	ns
			5.5 V		22	47		72		60	
	A or B	B or A	4.5 V		22	44		70		55	
			5.5 V		20	39		60		50	
	SBA or SAB†	A or B	4.5 V		26	55		83		69	
			5.5 V		24	49		74		62	
t_{en}	\overline{OEBA} or OEAB	A or B	4.5 V		33	66		100		82	ns
			5.5 V		30	59		90		74	
t_t		Any	4.5 V		17	42		63		53	ns
			5.5 V		14	38		57		48	

† These parameters are measured with the internal output state of the storage register opposite that of the bus input.

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	50	pF

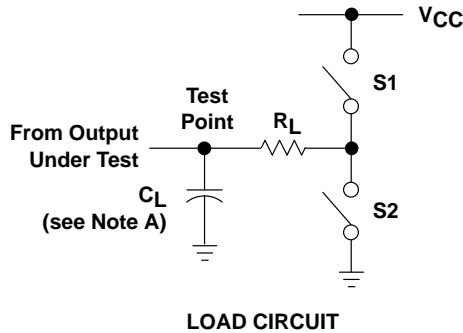
PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



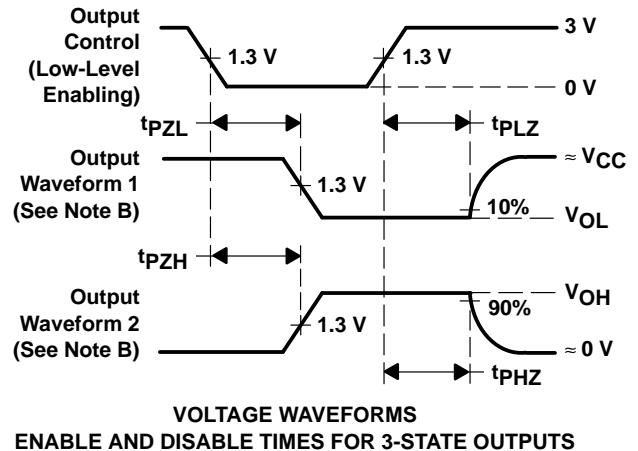
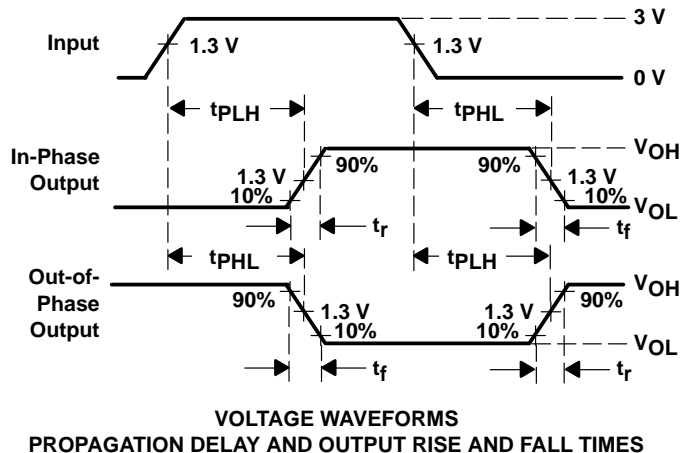
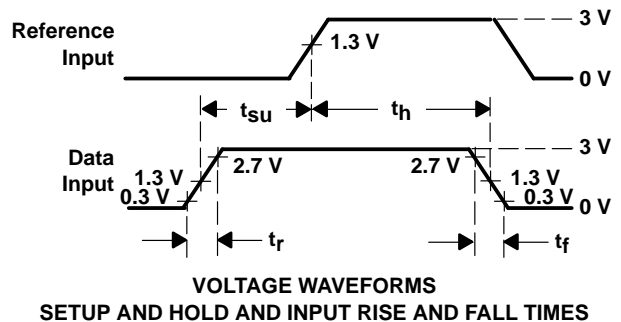
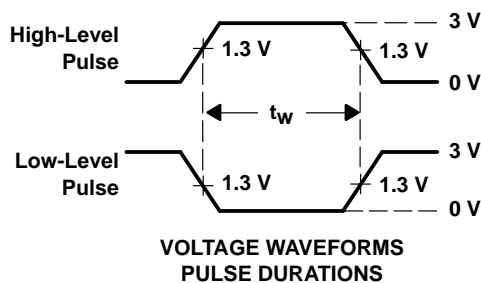
SN54HCT652, SN74HCT652 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SCLS179A – MARCH 1984 – REVISED JANUARY 1996

PARAMETER MEASUREMENT INFORMATION



PARAMETER	R_L	C_L	S1	S2
t_{en}	1 k Ω	50 pF or 150 pF	Open	Closed
			Closed	Open
t_{dis}	1 k Ω	50 pF	Open	Closed
			Closed	Open
t_{pd} or t_t	—	50 pF or 150 pF	Open	Open



- NOTES:
- A. C_L includes probe and test-fixture capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r = 6$ ns, $t_f = 6$ ns.
 - D. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
 - E. The outputs are measured one at a time with one input transition per measurement.
 - F. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - G. t_{PZL} and t_{PZH} are the same as t_{en} .
 - H. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.