

SN54AHC74, SN74AHC74 DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH CLEAR AND PRESET

SCLS255B – DECEMBER 1995 – REVISED JULY 1996

- Operating Range 2-V to 5.5-V V_{CC}
- **EPIC™** (Enhanced-Performance Implanted CMOS) Process
- High Latch-Up Immunity Exceeds 250 mA Per JEDEC Standard JESD-17
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

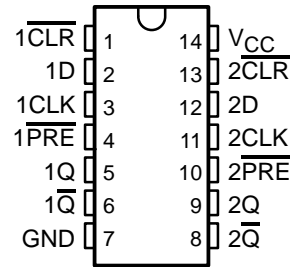
description

The 'AHC74 are dual positive-edge-triggered D-type flip-flops.

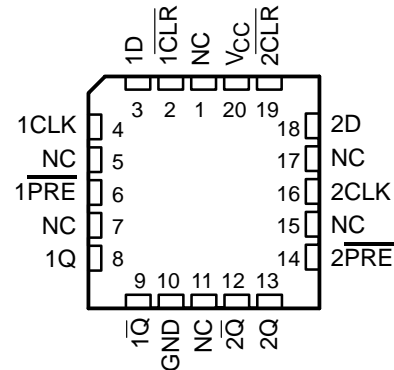
A low level at the preset (\overline{PRE}) or clear (\overline{CLR}) inputs sets or resets the outputs, regardless of the levels of the other inputs. When \overline{PRE} and \overline{CLR} are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

The SN54AHC74 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74AHC74 is characterized for operation from -40°C to 85°C .

SN54AHC74 . . . J OR W PACKAGE
SN74AHC74 . . . D, DB, N, OR PW PACKAGE
(TOP VIEW)



SN54AHC74 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE

INPUTS				OUTPUTS	
PRE	CLR	CLK	D	Q	Q̄
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H†	H†
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q ₀	Q̄ ₀

† This configuration is nonstable; that is, it does not persist when PRE or CLR returns to its inactive (high) level.



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Timing diagram for the 74VHC163 4-bit binary counter. The diagram shows two clock inputs, 1CLK and 2CLK, and two data inputs, 1D and 2D. The outputs are 1Q, 1Q-bar, 2Q, and 2Q-bar. The counter is shown in two states: 0000 and 0001. The timing shows that the counter increments on the rising edge of the clock inputs. The output 1Q-bar is the complement of 1Q, and 2Q-bar is the complement of 2Q.

Pin numbers shown are for the D, DB, J, N, PW, and W packages.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Output voltage range, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2): D package	1.25 W
DB or PW package	0.5 W
N package	1.1 W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

			SN54AHC74		SN74AHC74		UNIT
			MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage		2	5.5	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5		1.5		V
		V _{CC} = 3 V	2.1		2.1		
		V _{CC} = 5.5 V	3.85		3.85		
V _{IL}	Low-level input voltage	V _{CC} = 2 V	0.5		0.5		V
		V _{CC} = 3 V	0.9		0.9		
		V _{CC} = 5.5 V	1.65		1.65		
V _I	Input voltage		0	5.5	0	5.5	V
V _O	Output voltage		0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2 V	−50		−50		μA
		V _{CC} = 3.3 V ± 0.3 V	−4		−4		mA
		V _{CC} = 5 V ± 0.5 V	−8		−8		
I _{OL}	Low-level output current	V _{CC} = 2 V	50		50		μA
		V _{CC} = 3.3 V ± 0.3 V	4		4		mA
		V _{CC} = 5 V ± 0.5 V	8		8		
Δt/Δv	Input transition rise or fall rate	V _{CC} = 3.3 V ± 0.3 V	100		100		ns/V
		V _{CC} = 5 V ± 0.5 V	20		20		
T _A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54AHC74		SN74AHC74		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}		I _{OH} = -50 µA	2 V	1.9	2		1.9		1.9		V
			3 V	2.9	3		2.9		2.9		
			4.5 V	4.4	4.5		4.4		4.4		
		I _{OH} = -4 mA	3 V	2.58			2.48		2.48		
		I _{OH} = -8 mA	4.5 V	3.94			3.8		3.8		
V _{OL}		I _{OL} = 50 µA	2 V			0.1			0.1		V
			3 V			0.1			0.1		
			4.5 V			0.1			0.1		
		I _{OL} = 4 mA	3 V			0.36			0.5		
		I _{OL} = 8 mA	4.5 V			0.36			0.5		
I _I	Data inputs	V _I = V _{CC} or GND	5.5 V			±0.1			±1		µA
	Control inputs					±0.1			±1		
I _{CC}		V _I = V _{CC} or GND, I _O = 0	5.5 V			2			20		µA
C _i		V _I = V _{CC} or GND	5 V		2	10				10	pF

**timing requirements over recommended operating free-air temperature range,
V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

			T _A = 25°C		SN54AHC74		SN74AHC74		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ low	6		7		7		ns
		CLK	6		7		7		
t _{su}	Setup time before CLK↑	Data	6		7		7		ns
		$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ inactive	5		5		5		
t _h	Hold time, data after CLK↑		0.5		0.5		0.5		ns

**timing requirements over recommended operating free-air temperature range,
V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

			T _A = 25°C		SN54AHC74		SN74AHC74		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ low	5		5		5		ns
		CLK	5		5		5		
t _{su}	Setup time before CLK↑	Data	5		5		5		ns
		$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ inactive	3		3		3		
t _h	Hold time, data after CLK↑		0.5		0.5		0.5		ns



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switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN54AHC74					UNIT
				T _A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
f _{max}			C _L = 15 pF	80	125		70		MHz
			C _L = 50 pF	50	75		45		
t _{PLH} *	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$	Q or $\overline{\text{Q}}$	C _L = 15 pF	7.6	12.3		1	14.5	ns
t _{PHL} *				7.6	12.3		1	14.5	
t _{PLH} *	CLK	Q or $\overline{\text{Q}}$	C _L = 15 pF	6.7	11.9		1	14	ns
t _{PHL} *				6.7	11.9		1	14	
t _{PLH}	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$	Q or $\overline{\text{Q}}$	C _L = 50 pF	10.1	15.8		1	18	ns
t _{PHL}				10.1	15.8		1	18	
t _{PLH}	CLK	Q or $\overline{\text{Q}}$	C _L = 50 pF	9.2	15.4		1	17.5	ns
t _{PHL}				9.2	15.4		1	17.5	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN74AHC74					UNIT
				T _A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
f _{max}			C _L = 15 pF	80	125		70		MHz
			C _L = 50 pF	50	75		45		
t _{PLH}	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$	Q or $\overline{\text{Q}}$	C _L = 15 pF	7.6	12.3		1	14.5	ns
t _{PHL}				7.6	12.3		1	14.5	
t _{PLH}	CLK	Q or $\overline{\text{Q}}$	C _L = 15 pF	6.7	11.9		1	14	ns
t _{PHL}				6.7	11.9		1	14	
t _{PLH}	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$	Q or $\overline{\text{Q}}$	C _L = 50 pF	10.1	15.8		1	18	ns
t _{PHL}				10.1	15.8		1	18	
t _{PLH}	CLK	Q or $\overline{\text{Q}}$	C _L = 50 pF	9.2	15.4		1	17.5	ns
t _{PHL}				9.2	15.4		1	17.5	



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switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN54AHC74				UNIT	
				T _A = 25°C			MIN		MAX
				MIN	TYP	MAX			
f _{max}			C _L = 15 pF	130	170	110	MHz		
			C _L = 50 pF	90	115	75			
t _{PLH} *	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$	Q or $\overline{\text{Q}}$	C _L = 15 pF	4.8	7.7	1	9	ns	
t _{PHL} *				4.8	7.7	1	9		
t _{PLH} *	CLK	Q or $\overline{\text{Q}}$	C _L = 15 pF	4.6	7.3	1	8.5	ns	
t _{PHL} *				4.6	7.3	1	8.5		
t _{PLH}	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$	Q or $\overline{\text{Q}}$	C _L = 50 pF	6.3	9.7	1	11	ns	
t _{PHL}				6.3	9.7	1	11		
t _{PLH}	CLK	Q or Q	C _L = 50 pF	6.1	9.3	1	10.5	ns	
t _{PHL}				6.1	9.3	1	10.5		

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN74AHC74				UNIT	
				T _A = 25°C			MIN		MAX
				MIN	TYP	MAX			
f _{max}			C _L = 15 pF	130	170	110	MHz		
			C _L = 50 pF	90	115	75			
t _{PLH}	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$	Q or $\overline{\text{Q}}$	C _L = 15 pF	4.8	7.7	1	9	ns	
t _{PHL}				4.8	7.7	1	9		
t _{PLH}	CLK	Q or $\overline{\text{Q}}$	C _L = 15 pF	4.6	7.3	1	8.5	ns	
t _{PHL}				4.6	7.3	1	8.5		
t _{PLH}	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$	Q or $\overline{\text{Q}}$	C _L = 50 pF	6.3	9.7	1	11	ns	
t _{PHL}				6.3	9.7	1	11		
t _{PLH}	CLK	Q or Q	C _L = 50 pF	6.1	9.3	1	10.5	ns	
t _{PHL}				6.1	9.3	1	10.5		

noise characteristics, $V_{CC} = 5\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 4)

PARAMETER		SN74AHC74		UNIT
		MIN	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}	0.8		V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}	4.7	–0.8	V
$V_{IH(D)}$	High-level dynamic input voltage	3.5		V
$V_{IL(D)}$	Low-level dynamic input voltage	1.5		V

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

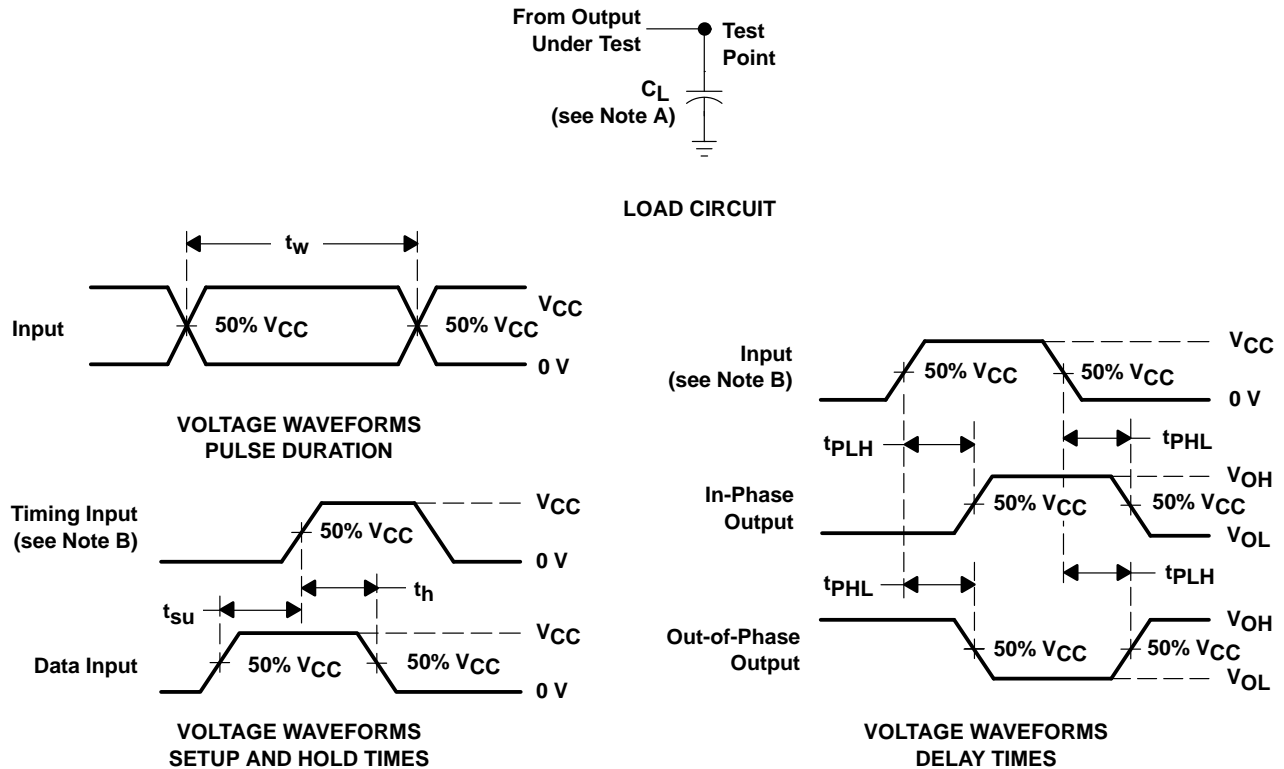
PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance No load, $f = 1\text{ MHz}$	32	pF



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PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r = 3$ ns, $t_f = 3$ ns.
 C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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