

# SN54AHCT16373, SN74AHCT16373 16-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCLS336A – MARCH 1996 – REVISED NOVEMBER 1996

- Members of the Texas Instruments **Widebus™** Family
- Inputs Are TTL-Voltage Compatible
- **EPIC™** (Enhanced-Performance Implanted CMOS) Process
- Distributed  $V_{CC}$  and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

## description

The 'AHCT16373 are 16-bit transparent D-type latches with 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

These devices can be used as two 8-bit latches or one 16-bit latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

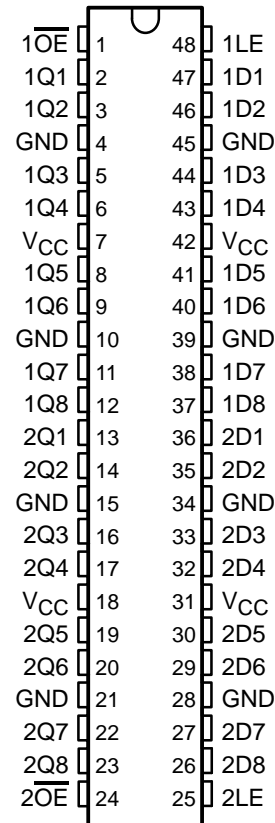
A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{OE}$  does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74AHCT16373 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54AHCT16373 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74AHCT16373 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

SN54AHCT16373 . . . WD PACKAGE  
SN74AHCT16373 . . . DGG OR DL PACKAGE  
(TOP VIEW)



PRODUCT PREVIEW



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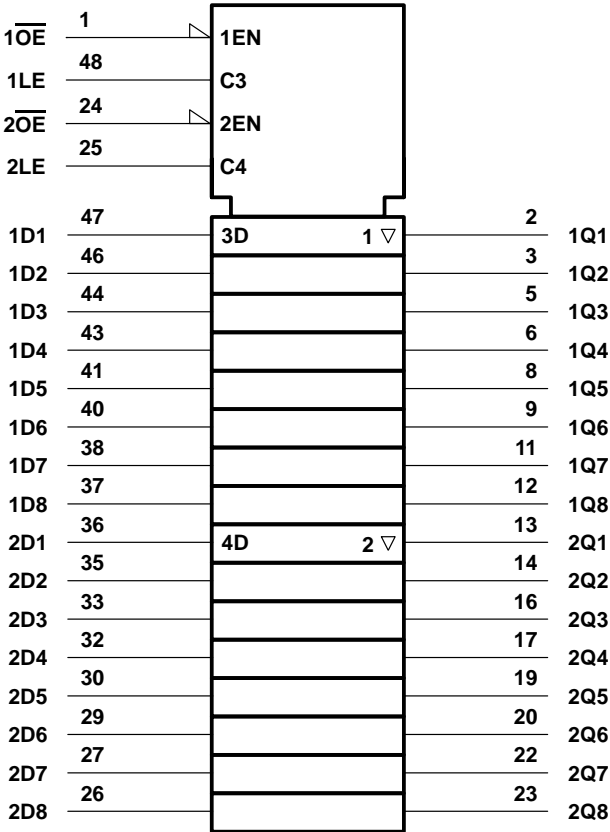
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FUNCTION TABLE  
(each latch)

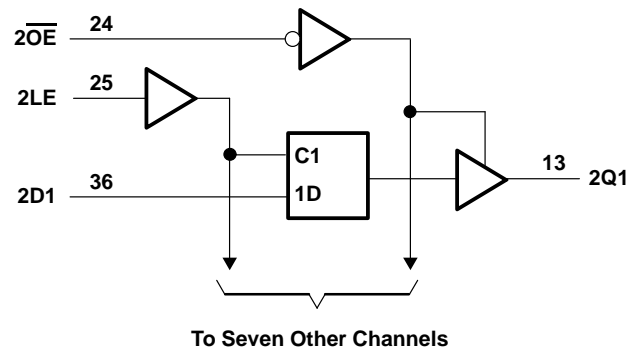
INPUTS			OUTPUT Q
$\overline{\text{OE}}$	LE	D	
L	H	H	H
L	H	L	L
L	L	X	$Q_0$
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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Supply voltage range, $V_{CC}$	.....	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	.....	-0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1)	.....	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ )	.....	-20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	.....	-20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	.....	$\pm 25$ mA
Continuous current through each $V_{CC}$ or GND	.....	$\pm 75$ mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2):		
	DGG package	0.85 W
	DL package	1.2 W
Storage temperature range, $T_{stg}$	.....	$-65^\circ\text{C}$ to $150^\circ\text{C}$

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

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#### recommended operating conditions (see Note 3)

		SN54AHCT16373		SN74AHCT16373		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	4.5	5.5	4.5	5.5	V
$V_{IH}$	High-level input voltage	2		2		V
$V_{IL}$	Low-level input voltage		0.8		0.8	V
$V_I$	Input voltage	0	5.5	0	5.5	V
$V_O$	Output voltage	0	$V_{CC}$	0	$V_{CC}$	V
$I_{OH}$	High-level output current		–8		–8	mA
$I_{OL}$	Low-level output current		8		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20		20	ns/V
$T_A$	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$V_{CC}$	$T_A = 25^\circ\text{C}$			SN54AHCT16373		SN74AHCT16373		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$V_{OH}$	$I_{OH} = -50\ \mu\text{A}$	4.5 V	4.4	4.5		4.4		4.4		V
	$I_{OH} = -8\ \text{mA}$		3.94			3.8		3.8		
$V_{OL}$	$I_{OL} = 50\ \mu\text{A}$	4.5 V			0.1		0.1		0.1	V
	$I_{OL} = 8\ \text{mA}$				0.36		0.44		0.44	
$I_{OZ}$	$V_O = V_{CC}$ or GND	5.5 V			$\pm 0.25$		$\pm 2.5$		$\pm 2.5$	$\mu\text{A}$
$I_I$	$V_I = V_{CC}$ or GND	5.5 V			$\pm 0.1$		$\pm 1$		$\pm 1$	$\mu\text{A}$
$I_{CC}$	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			4		40		40	$\mu\text{A}$
$\Delta I_{CC}^\dagger$	One input at 3.4 V, Other inputs at $V_{CC}$ or GND	5.5 V			1.35		1.5		1.5	mA
$C_i$	$V_I = V_{CC}$ or GND	5 V		4						pF
$C_o$	$V_O = V_{CC}$ or GND	5 V		6						pF

$^\dagger$  This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or  $V_{CC}$ .

#### timing requirements over recommended operating free-air temperature range, $V_{CC} = 5\ \text{V} \pm 0.5\ \text{V}$ (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ\text{C}$		SN54AHCT16373		SN74AHCT16373		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_w$	Pulse duration, $\overline{LE}$ high	6.5		6.5		6.5		ns
$t_{su}$	Setup time, data before $\overline{LE}\downarrow$	1.5		1.5		1.5		ns
$t_h$	Hold time, data after $\overline{LE}\downarrow$	3.5		3.5		3.5		ns

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switching characteristics over recommended operating free-air temperature range,  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54AHCT16373		SN74AHCT16373		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}^*$	D	Q	$C_L = 15\text{ pF}$	5.1	8.5		1	9.5	1	9.5	ns
$t_{PHL}^*$				5.1	8.5		1	9.5	1	9.5	
$t_{PLH}^*$	LE	Q	$C_L = 15\text{ pF}$	7.7	12.3		1	13.5	1	13.5	ns
$t_{PHL}^*$				7.7	12.3		1	13.5	1	13.5	
$t_{PZH}^*$	$\overline{OE}$	Q	$C_L = 15\text{ pF}$	6.3	10.9		1	12.5	1	12.5	ns
$t_{PZL}^*$				6.3	10.9		1	12.5	1	12.5	
$t_{PHZ}^*$	$\overline{OE}$	Q	$C_L = 15\text{ pF}$	6	10.2		1	11	1	11	ns
$t_{PLZ}^*$				6	10.2		1	11	1	11	
$t_{PLH}$	D	Q	$C_L = 50\text{ pF}$	5.9	9.5		1	10.5	1	10.5	ns
$t_{PHL}$				5.9	9.5		1	10.5	1	10.5	
$t_{PLH}$	LE	Q	$C_L = 50\text{ pF}$	8.5	13.3		1	14.5	1	14.5	ns
$t_{PHL}$				8.5	13.3		1	14.5	1	14.5	
$t_{PZH}$	$\overline{OE}$	Q	$C_L = 50\text{ pF}$	7.1	11.9		1	13.5	1	13.5	ns
$t_{PZL}$				7.1	11.9		1	13.5	1	13.5	
$t_{PHZ}$	$\overline{OE}$	Q	$C_L = 50\text{ pF}$	6.8	11.2		1	12	1	12	ns
$t_{PLZ}$				6.8	11.2		1	12	1	12	

\* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

output-skew characteristics,  $C_L = 50\text{ pF}$  (see Note 4)

PARAMETER		V <sub>CC</sub>	SN74AHCT16373				UNIT
			T <sub>A</sub> = 25°C		MIN    MAX		
			MIN	MAX			
t <sub>sk(o)</sub>	Output skew	5 V ± 0.5 V	1		1		ns

NOTE 4: Characteristics are determined during product characterization and ensured by design.

noise characteristics,  $V_{CC} = 5\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$  (see Note 5)

PARAMETER		SN74AHCT16373			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic $V_{OL}$		0.8	1.2	V
$V_{OL(V)}$	Quiet output, minimum dynamic $V_{OL}$		-0.8	-1.2	V
$V_{OH(V)}$	Quiet output, minimum dynamic $V_{OH}$		4.1		V
$V_{IH(D)}$	High-level dynamic input voltage		2		V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

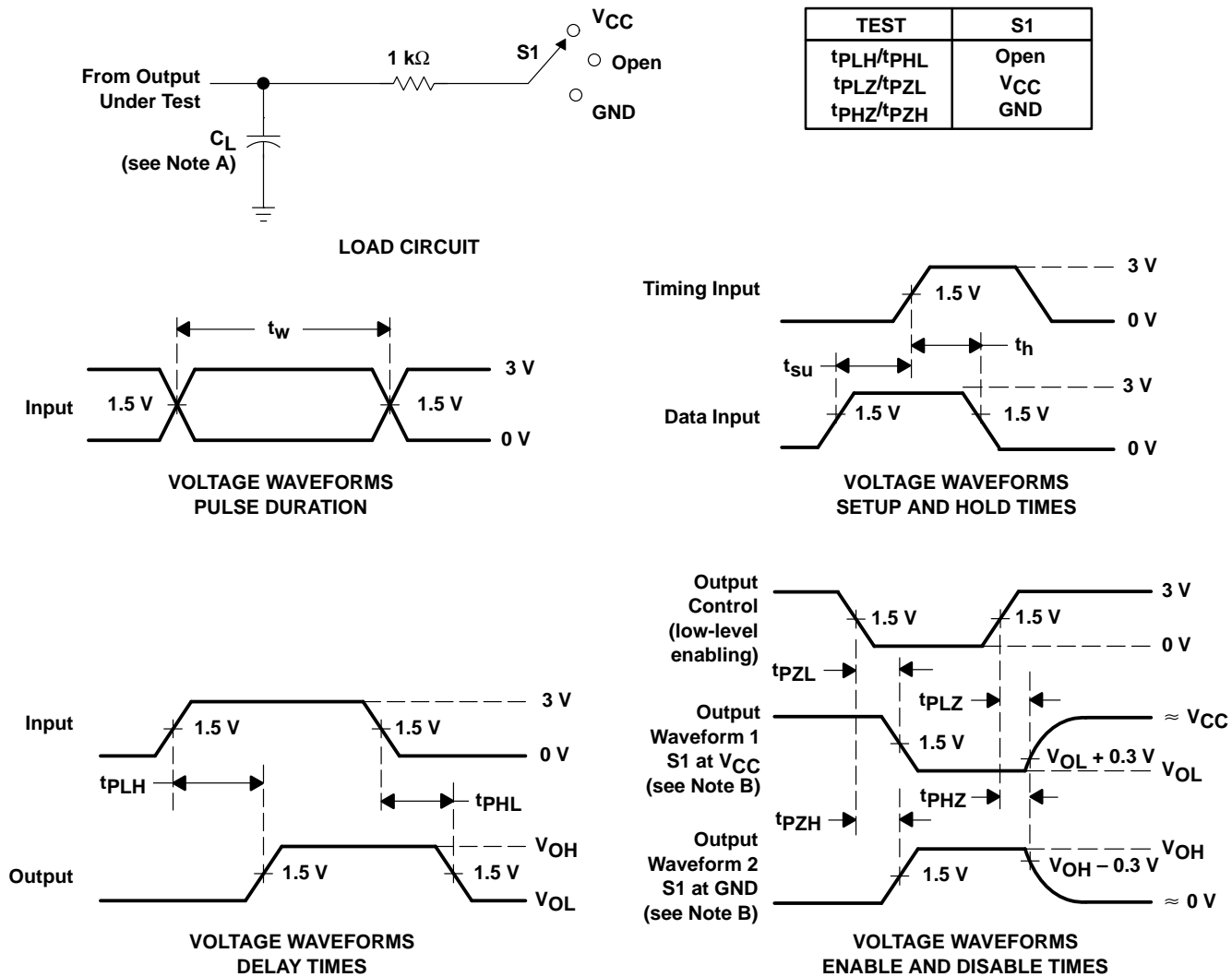
PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance	No load, $f = 1\text{ MHz}$	17	pF

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PARAMETER MEASUREMENT INFORMATION



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