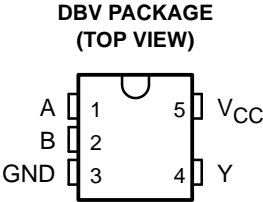


# SN74AHCT1G02

## SINGLE 2-INPUT POSITIVE-NOR GATE

SCLS341B – APRIL 1996 – REVISED NOVEMBER 1996

- Inputs Are TTL-Voltage Compatible
- **EPIC™** (Enhanced-Performance Implanted CMOS) Process
- Packaged in Plastic Small-Outline Transistor Package



### description

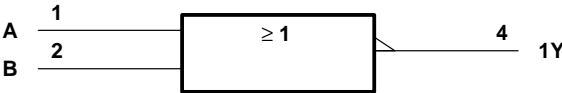
This device contains a single 2-input NOR gate that performs the Boolean function  $Y = \overline{A} \cdot \overline{B}$  or  $Y = \overline{A + B}$  in positive logic.

The SN74AHCT1G02 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

FUNCTION TABLE

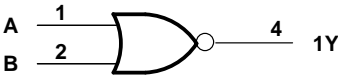
INPUTS		OUTPUTS
A	B	Y
H	X	L
X	H	L
L	L	H

### logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

### logic diagram (positive logic)



PRODUCT PREVIEW



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# SN74AHCT1G02

## SINGLE 2-INPUT POSITIVE-NOR GATE

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### absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	–20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±25 mA
Continuous current through $V_{CC}$ or GND	±50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2)	0.2 W
Storage temperature range, $T_{stg}$	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 25 millimeters.

### recommended operating conditions (see Note 3)

	MIN	MAX	UNIT
$V_{CC}$ Supply voltage	4.5	5.5	V
$V_{IH}$ High-level input voltage	2		V
$V_{IL}$ Low-level input voltage		0.8	V
$V_I$ Input voltage	0	5.5	V
$V_O$ Output voltage	0	$V_{CC}$	V
$I_{OH}$ High-level output current		–8	mA
$I_{OL}$ Low-level output current		8	mA
$\Delta t/\Delta v$ Input transition rise or fall rate		20	ns/V
$T_A$ Operating free-air temperature	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$V_{CC}$	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
$V_{OH}$	$I_{OH} = -50 \mu\text{A}$	4.5 V	4.4	4.5		4.4		V
	$I_{OH} = -8 \text{ mA}$		3.94			3.8		
$V_{OL}$	$I_{OL} = 50 \mu\text{A}$	4.5 V			0.1	0.1		V
	$I_{OL} = 8 \text{ mA}$				0.36	0.44		
$I_I$	$V_I = V_{CC}$ or GND	5.5 V			±0.1	±1		μA
$I_{CC}$	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			2	20		μA
$\Delta I_{CC}^\ddagger$	One input at 3.4 V, Other inputs at GND or $V_{CC}$	5.5 V			1.35	1.5		mA
$C_i$	$V_I = V_{CC}$ or GND	5 V			4	10	10	pF

‡ This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or  $V_{CC}$ .

PRODUCT PREVIEW



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## SINGLE 2-INPUT POSITIVE-NOR GATE

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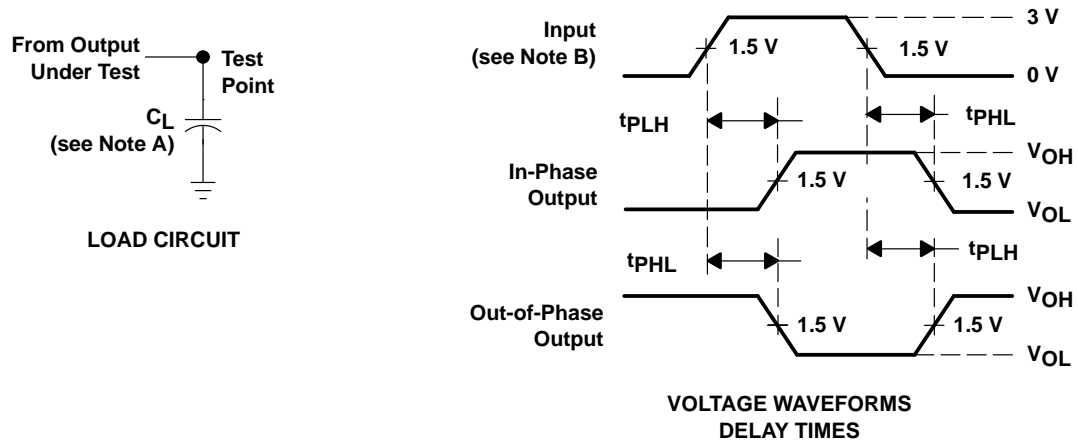
switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			UNIT
				MIN	TYP	MAX	
$t_{PLH}$	A or B	Y	$C_L = 15\text{ pF}$			1	ns
$t_{PHL}$						1	
$t_{PLH}$	A or B	Y	$C_L = 50\text{ pF}$			1	ns
$t_{PHL}$						1	

operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance	No load, $f = 1\text{ MHz}$	17	pF

### PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r = 3\text{ ns}$ ,  $t_f = 3\text{ ns}$ .  
 C. The output is measured with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

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