

# SN54ALS874B, SN74ALS874B, SN74ALS876A SN74AS874, SN74AS876 DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS

SDAS061C – APRIL 1982 – REVISED JANUARY 1995

- 3-State Buffer-Type Outputs Drive Bus Lines Directly
- Bus-Structured Pinout
- Choice of True or Inverting Logic
  - SN54ALS874B, SN74ALS874B, SN74AS874 Have True Outputs
  - SN74ALS876A, SN74AS876 Have Inverting Outputs
- Asynchronous Clear
- Package Options Include Plastic Small-Outline (DW) Packages, Plastic (FN) and Ceramic (FK) Chip Carriers, and Standard Plastic (NT) and Ceramic (JT) 300-mil DIPs

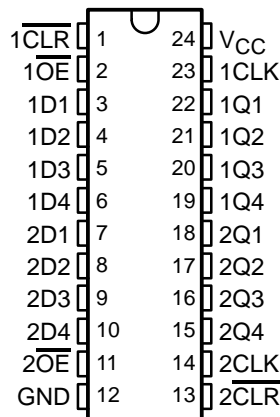
## description

These dual 4-bit D-type edge-triggered flip-flops feature 3-state outputs designed specifically as bus drivers. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

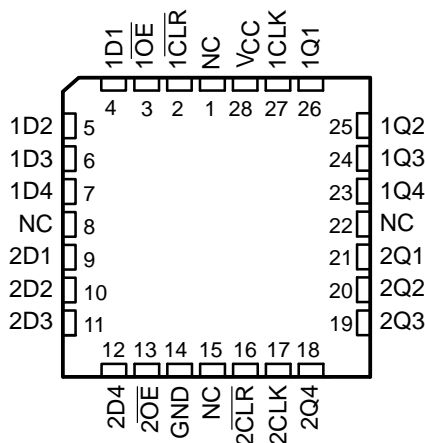
The edge-triggered flip-flops enter data on the low-to-high transition of the clock (CLK) input. The SN54ALS874B, SN74ALS874B, and SN74AS874 have clear ( $\overline{\text{CLR}}$ ) inputs and noninverting Q outputs. The SN74ALS876A and SN74AS876 have preset ( $\overline{\text{PRE}}$ ) inputs and inverting  $\overline{\text{Q}}$  outputs; taking  $\overline{\text{PRE}}$  low causes the four Q or  $\overline{\text{Q}}$  outputs to go low independently of the clock.

The SN54ALS874B is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74ALS874B, SN74ALS876A, SN74AS874, and SN74AS876 devices are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

SN54ALS874B . . . JT PACKAGE  
SN74ALS874B, SN74AS874 . . . DW OR NT PACKAGE  
(TOP VIEW)

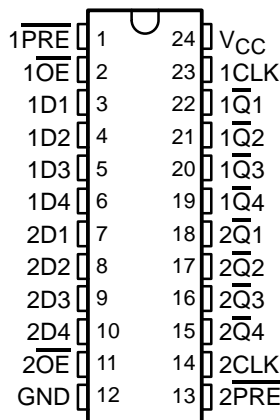


SN54ALS874B . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

SN74ALS876A, SN74AS876 . . . DW OR NT PACKAGE  
(TOP VIEW)



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## Function Tables

SN54ALS874B, SN74ALS874B, SN74AS874  
(each flip-flop)

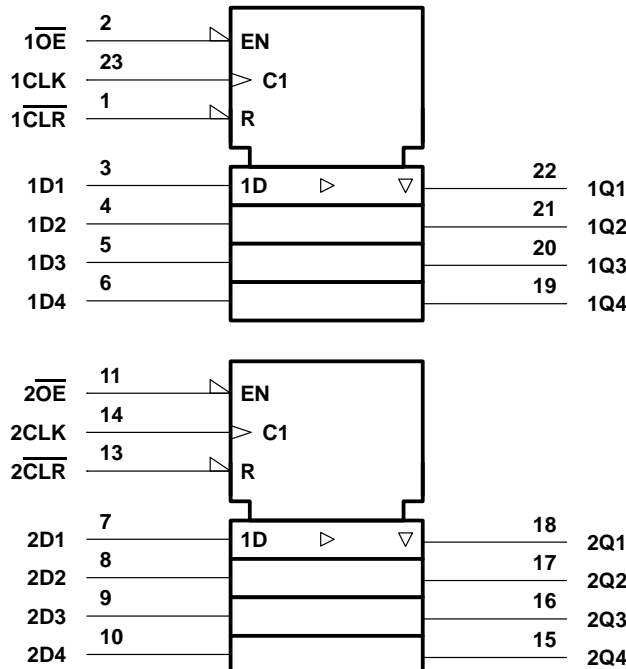
INPUTS				OUTPUT Q
$\overline{OE}$	$\overline{CLR}$	CLK	D	
L	L	X	X	L
L	H	↑	H	H
L	H	↑	L	L
L	H	L	X	Q <sub>0</sub>
H	X	X	X	Z

SN74ALS876A, SN74AS876  
(each flip-flop)

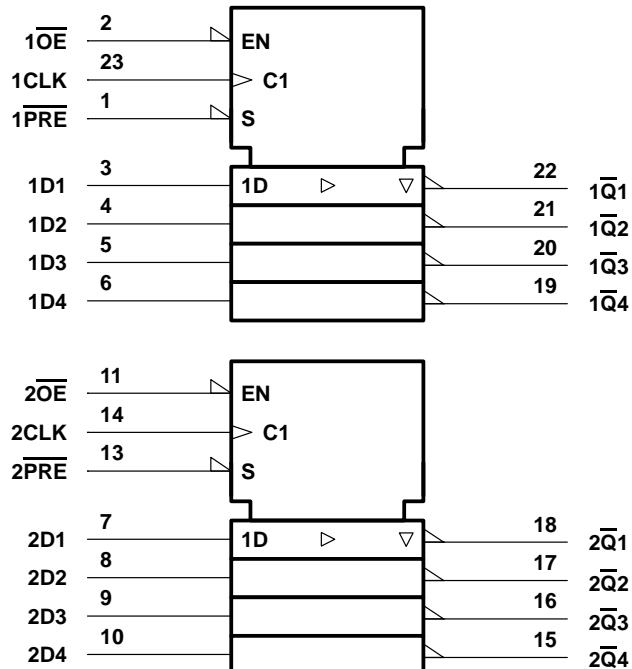
INPUTS				OUTPUT $\overline{Q}$
$\overline{OE}$	$\overline{PRE}$	CLK	D	
L	L	X	X	L
L	H	↑	H	L
L	H	↑	L	H
L	H	L	X	$\overline{Q_0}$
H	X	X	X	Z

## logic symbols†

SN54ALS874B, SN74ALS874B, SN74AS874

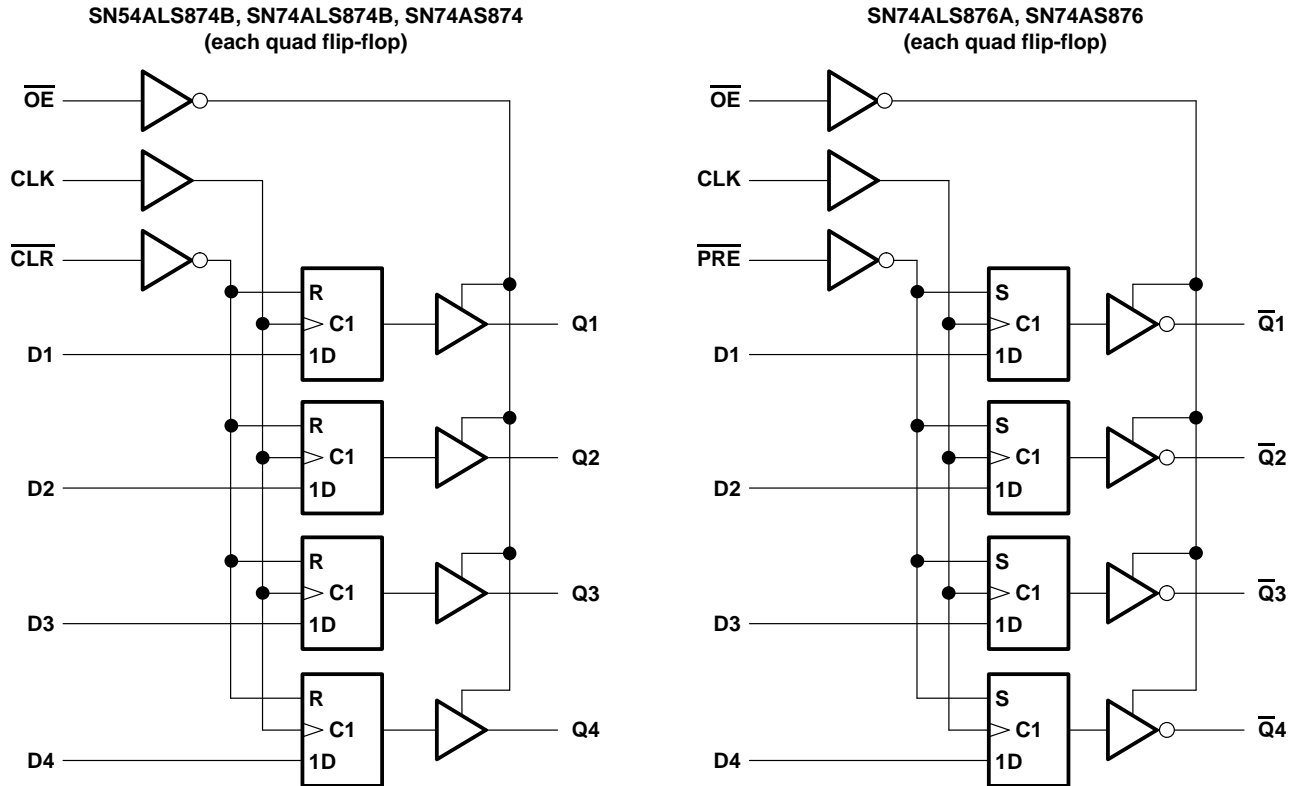


SN74ALS876A, SN74AS876



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.  
Pin numbers shown are for the DW, JT, and NT packages.

logic diagrams (positive logic)



Pin numbers shown are for the DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage, $V_{CC}$	7 V
Input voltage, $V_I$	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, $T_A$ : SN54ALS874B	–55°C to 125°C
SN74ALS874B, SN74ALS876A	0°C to 70°C
Storage temperature range	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**SN54ALS874B, SN74ALS874B, SN74ALS876A**  
**SN74AS874, SN74AS876**  
**DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS**

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**recommended operating conditions**

			SN54ALS874B			SN74ALS874B SN74ALS876A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V <sub>IH</sub>	High-level input voltage		2			2			V
V <sub>IL</sub>	Low-level input voltage				0.7			0.8	V
I <sub>OH</sub>	High-level output current				–1			–2.6	mA
I <sub>OL</sub>	Low-level output current				12			24	mA
f <sub>clock</sub>	Clock frequency		0		25	0		30	MHz
t <sub>w</sub>	Pulse duration	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ low	15			10			ns
		CLK high	20			16.5			
		CLK low	20			16.5			
t <sub>su</sub>	Setup time before CLK↑	Data	15			15			ns
		$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ inactive	15			10			
t <sub>h</sub>	Hold time, data after CLK↑		4			0			ns
T <sub>A</sub>	Operating free-air temperature		–55		125	0		70	°C

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS				SN54ALS874B			SN74ALS874B SN74ALS876A			UNIT
						MIN	TYP†	MAX	MIN	TYP†	MAX	
V <sub>IK</sub>		V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = –18 mA						–1.2			–1.2	V
V <sub>OH</sub>		V <sub>CC</sub> = 4.5 V to 5.5 V, I <sub>OH</sub> = –0.4 mA				V <sub>CC</sub> – 2			V <sub>CC</sub> – 2			V
		V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = –1 mA				2.4	3.3					
		V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = –2.6 mA							2.4	3.2		
V <sub>OL</sub>		V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 12 mA				0.25	0.4		0.25	0.4		V
		V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 24 mA							0.35	0.5		
I <sub>OZH</sub>		V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.7 V						20			20	μA
I <sub>OZL</sub>		V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0.4 V						–20			–20	μA
I <sub>I</sub>		V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 7 V						0.1			0.1	mA
I <sub>IH</sub>		V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 2.7 V						20			20	μA
I <sub>IL</sub>		V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 0.4 V						–0.2			–0.2	mA
I <sub>O‡</sub>		V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.25 V				–20		–112	–30		–112	mA
I <sub>CC</sub>	'ALS874B	V <sub>CC</sub> = 5.5 V	Outputs high			14	21		14	21		mA
			Outputs low			19	30		19	30		
			Outputs disabled			20	32		20	32		
	SN74ALS876A	V <sub>CC</sub> = 5.5 V	Outputs high						14	21		
			Outputs low						18	29		
			Outputs disabled						20	31		

† All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I<sub>OS</sub>.



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SN54ALS874B, SN74ALS874B, SN74ALS876A  
SN74AS874, SN74AS876  
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**switching characteristics (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T <sub>A</sub> = MIN to MAX†				UNIT
			SN54ALS874B		SN74ALS874B		
			MIN	MAX	MIN	MAX	
f <sub>max</sub>			25		30		MHz
t <sub>PLH</sub>	CLK	Any Q	4	18	4	14	ns
t <sub>PHL</sub>			4	16	4	14	
t <sub>PHL</sub>	$\overline{\text{CLR}}$	Any Q	5	23	5	17	ns
t <sub>PZH</sub>	$\overline{\text{OE}}$	Any Q	4	24	4	18	ns
t <sub>PZL</sub>			4	21	4	18	
t <sub>PHZ</sub>	$\overline{\text{OE}}$	Any Q	2	15	2	10	ns
t <sub>PLZ</sub>			3	22	3	12	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

**switching characteristics (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R <sub>1</sub> = 500 Ω, R <sub>2</sub> = 500 Ω, T <sub>A</sub> = MIN to MAX†		UNIT
			SN74ALS876A		
			MIN	MAX	
f <sub>max</sub>			30		MHz
t <sub>PLH</sub>	CLK	Any $\overline{Q}$	4	14	ns
t <sub>PHL</sub>			4	14	
t <sub>PHL</sub>	$\overline{PRE}$	Any $\overline{Q}$	6	19	ns
t <sub>PZH</sub>	$\overline{OE}$	Any $\overline{Q}$	4	18	ns
t <sub>PZL</sub>			4	18	
t <sub>PHZ</sub>	$\overline{OE}$	Any $\overline{Q}$	2	10	ns
t <sub>PLZ</sub>			3	13	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡**

Supply voltage, V <sub>CC</sub>	7 V
Input voltage, V <sub>I</sub>	7 V
Operating free-air temperature range, T <sub>A</sub> : SN74AS874, SN74AS876	0°C to 70°C
Storage temperature range	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**SN54ALS874B, SN74ALS874B, SN74ALS876A**  
**SN74AS874, SN74AS876**  
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**recommended operating conditions**

			SN74AS874			SN74AS876			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V <sub>IH</sub>	High-level input voltage		2			2			V
V <sub>IL</sub>	Low-level input voltage		0.8			0.8			V
I <sub>OH</sub>	High-level output current		−15			−15			mA
I <sub>OL</sub>	Low-level output current		48			48			mA
f <sub>clock</sub>	Clock frequency		0	125		0	80		MHz
t <sub>w</sub>	Pulse duration	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ low	2			4.5			ns
		CLK high	3			6.2			
		CLK low	4			6.2			
t <sub>su</sub>	Setup time before CLK↑	Data	2			4.5			ns
		$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ inactive	4			5			
t <sub>h</sub>	Hold time, data after CLK↑		1			2			ns
T <sub>A</sub>	Operating free-air temperature		0	70		0	70		°C

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS		SN74AS874 SN74AS876			UNIT
				MIN	TYP†	MAX	
V <sub>IK</sub>		V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = −18 mA	−1.2			V
V <sub>OH</sub>		V <sub>CC</sub> = 4.5 V to 5.5 V,	I <sub>OH</sub> = −2 mA	V <sub>CC</sub> − 2			V
		V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = −15 mA	2.4	3.3		
V <sub>OL</sub>		V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 48 mA	0.35	0.5		V
I <sub>OZH</sub>		V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V	50			μA
I <sub>OZL</sub>		V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.4 V	−50			μA
I <sub>I</sub>		V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 7 V	0.1			mA
I <sub>IH</sub>		V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 2.7 V	20			μA
I <sub>IL</sub>	D	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 0.4 V	−2			mA
	All others			−0.5			
I <sub>O†</sub>		V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.25 V	−30	−112		mA
I <sub>CC</sub>	SN74AS874	V <sub>CC</sub> = 5.5 V	Outputs high	82	133		mA
			Outputs low	92	149		
			Outputs disabled	100	160		
	SN74AS876	V <sub>CC</sub> = 5.5 V	Outputs high	88	142		
			Outputs low	94	150		
			Outputs disabled	100	160		

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .



SN54ALS874B, SN74ALS874B, SN74ALS876A  
 SN74AS874, SN74AS876  
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**switching characteristics (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T <sub>A</sub> = MIN to MAX†		UNIT
			SN74AS874		
			MIN	MAX	
f <sub>max</sub>			125		MHz
t <sub>PLH</sub>	CLK	Any Q	3	8.5	ns
t <sub>PHL</sub>			4	10.5	
t <sub>PHL</sub>	$\overline{\text{CLR}}$	Any Q	4	9.5	ns
t <sub>PZH</sub>	$\overline{\text{OE}}$	Any Q	2	7	ns
t <sub>PZL</sub>			3	10.5	
t <sub>PHZ</sub>	$\overline{\text{OE}}$	Any Q	2	6	ns
t <sub>PLZ</sub>			2	7.5	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

**switching characteristics (see Figure 1)**

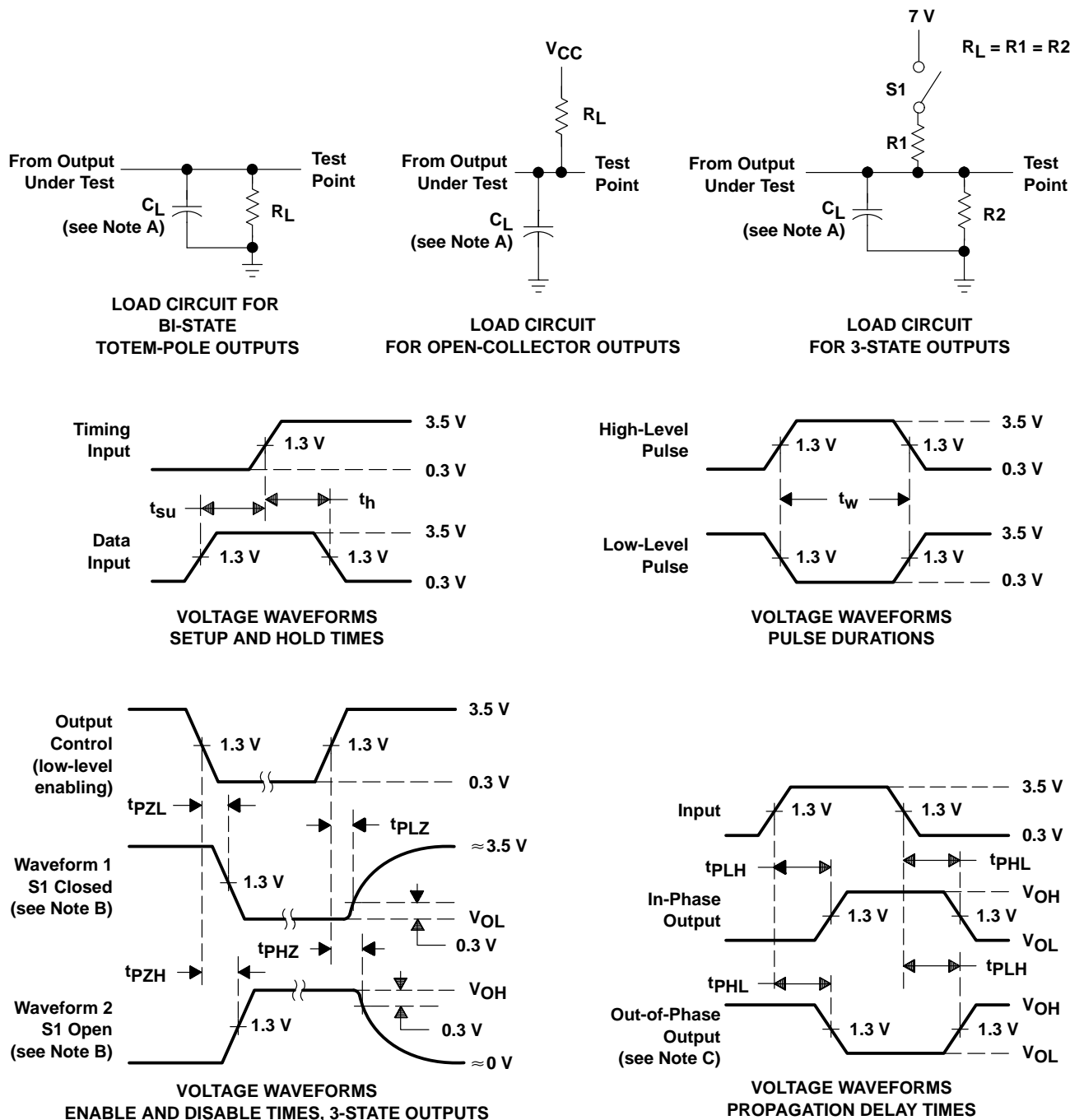
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T <sub>A</sub> = MIN to MAX†		UNIT
			SN74AS876		
			MIN	MAX	
f <sub>max</sub>			80		MHz
t <sub>PLH</sub>	CLK	Any $\overline{\text{Q}}$	3	8.5	ns
t <sub>PHL</sub>			4	10.5	
t <sub>PHL</sub>	$\overline{\text{PRE}}$	Any $\overline{\text{Q}}$	4	9.5	ns
t <sub>PZH</sub>	$\overline{\text{OE}}$	Any $\overline{\text{Q}}$	2	7	ns
t <sub>PZL</sub>			3	11	
t <sub>PHZ</sub>	$\overline{\text{OE}}$	Any $\overline{\text{Q}}$	2	7	ns
t <sub>PLZ</sub>			2	7	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

**SN54ALS874B, SN74ALS874B, SN74ALS876A**  
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**DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS**

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**PARAMETER MEASUREMENT INFORMATION**  
**SERIES 54ALS/74ALS AND 54AS/74AS DEVICES**



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.  
 D. All input pulses have the following characteristics:  $PRR \leq 1$  MHz,  $t_r = t_f = 2$  ns, duty cycle = 50%.  
 E. The outputs are measured one at a time with one transition per measurement.

**Figure 1. Load Circuits and Voltage Waveforms**



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