

SN54ALS880A, SN54AS880, SN74ALS880A, SN74AS880 DUAL 4-BIT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SDAS079A – D2661, DECEMBER 1982 – REVISED MAY 1986

- 3-State Buffer-Type Outputs Drive Bus Lines Directly
- Bus-Structured Pinout
- 'ALS873B is Alternative Version With Noninverting Outputs
- Package Options Include Plastic Small Outline Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These dual 4-bit registers feature 3-state outputs designed specifically for bus driving. This makes these devices particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The dual 4-bit latches are transparent D-type. When the latch enable input (1C or 2C) is high, the \bar{Q} outputs will follow the data (D) inputs in inverted form, according to the function table. When the latch enable input is taken low, the \bar{Q} outputs will be latched. When \overline{PRE} goes low, the \bar{Q} outputs go low independently of the clock. The outputs are in a high-impedance state when \overline{OC} (output control) is at a high logic level.

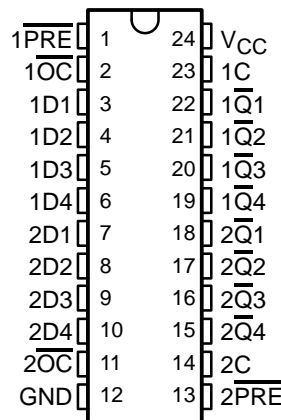
The SN54ALS880A and SN54AS880 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ALS880A and SN74AS880 are characterized for operation from 0°C to 70°C .

FUNCTION TABLE
(each latch)

INPUTS				OUTPUT \bar{Q}
\overline{OC}	\overline{PRE}	C	D	
L	L	X	X	L
L	H	H	H	L
L	H	H	L	H
L	H	L	X	\bar{Q}_0
H	X	X	X	Z

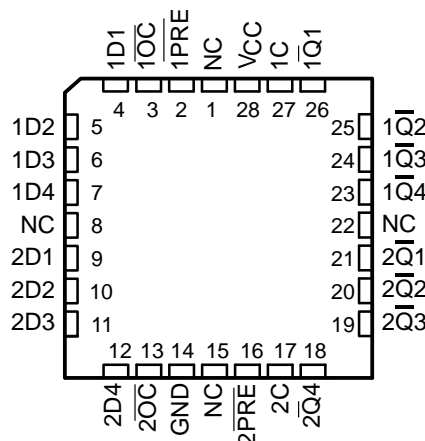
SN54ALS880A, SN54AS880 . . . JT PACKAGE
SN74ALS880A, SN74AS880 . . . DW OR NT PACKAGE

(TOP VIEW)



SN54ALS880A, SN54AS880 . . . JT PACKAGE
SN74ALS880A, SN74AS880 . . . DW OR NT PACKAGE

(TOP VIEW)



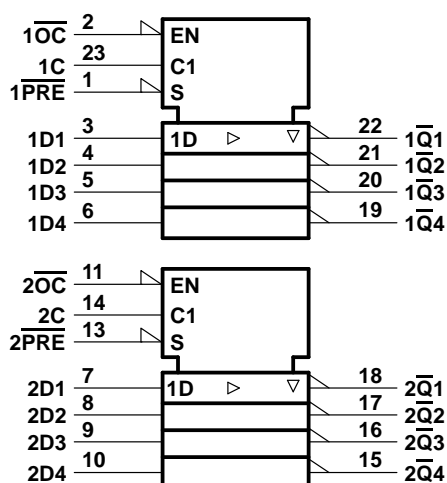
NC – No internal connection

SN54ALS880A, SN54AS880, SN74ALS880A, SN74AS880

DUAL 4-BIT D-TYPE LATCHES WITH 3-STATE OUTPUTS

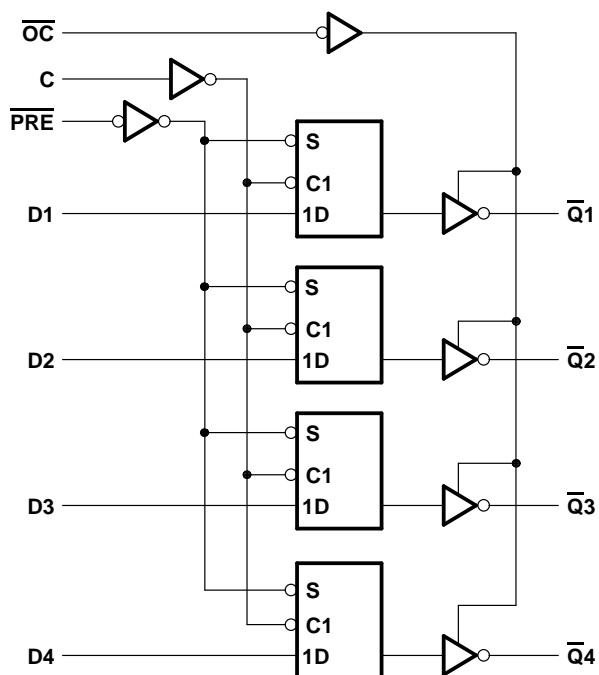
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

logic diagram (each quad latch, positive logic)



SN54ALS880A, SN54AS880, SN74ALS880A, SN74AS880 DUAL 4-BIT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	7 V
Input voltage	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range: SN54ALS880A, SN54AS880	–55°C to 125°C
SN74ALS880A, SN74AS880	0°C to 70°C
Storage temperature range	–65°C to 150°C

recommended operating conditions

			SN54ALS880A			SN74ALS880A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage		2			2			V
V _{IL}	Low-level input voltage		0.7			0.8			V
I _{OH}	High-level output current		−1			−2.6			mA
I _{OL}	Low-level output current		12			24			mA
t _w	Pulse duration	PRE low	15			15			ns
		C high	15			15			
t _{su}	Setup time, data before C↓		10			10			ns
t _h	Hold time, data after C↓		10			10			ns
T _A	Operating free-air temperature		−55 125			0 70			°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS880A			SN74ALS880A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{IK}	V _{CC} = 4.5 V,	I _I = −18 mA	−1.2			−1.2			V
V _{OH}	V _{CC} = 4.5 V to 5.5 V,	I _{OH} = −0.4 mA	V _{CC} − 2			V _{CC} − 2			V
	V _{CC} = 4.5 V,	I _{OH} = −1 mA	2.4	3.3					
	V _{CC} = 4.5 V,	I _{OH} = −2.6 mA				2.4	3.2		
V _{OL}	V _{CC} = 4.5 V,	I _{OL} = 12 mA	0.25 0.4			0.25 0.4			V
	V _{CC} = 4.5 V,	I _{OL} = 24 mA				0.35 0.5			
I _{OZH}	V _{CC} = 5.5 V,	V _O = 2.7 V	20			20			μA
I _{OZL}	V _{CC} = 5.5 V,	V _O = 0.4 V	−20			−20			μA
I _I	V _{CC} = 5.5 V,	V _I = 7 V	0.1			0.1			mA
I _{IH}	V _{CC} = 5.5 V,	V _I = 2.7 V	20			20			μA
I _{IL}	V _{CC} = 5.5 V,	V _I = 0.4 V	−0.2			−0.2			mA
I _O ‡	V _{CC} = 5.5 V,	V _O = 2.25 V	−30	−112		−30	−112		mA
I _{CC}	V _{CC} = 5.5 V	Outputs high	14 21		14 21				mA
		Outputs low	19 29		19 29				
		Outputs disabled	20 31		20 31				

† All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

SN54ALS880A, SN74ALS880A

DUAL 4-BIT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T _A = 25°C			V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T _A = MIN to MAX				UNIT
			'ALS880A			SN54ALS880A		SN74ALS880A		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	D	\overline{Q}	14	19		3	23	3	20	ns
t _{PHL}			9	12		3	15	3	14	
t _{PLH}	C	\overline{Q}	17	22		8	31	8	24	ns
t _{PHL}			14	18		8	22	8	21	
t _{PHL}	PRE	\overline{Q}	12	16		6	24	6	21	ns
t _{PZH}	\overline{OC}	\overline{Q}	12	15		4	21	4	18	ns
t _{PZL}			13	17		4	21	4	18	
t _{PHZ}	\overline{OC}	\overline{Q}	6	9		2	12	2	10	ns
t _{PLZ}			8	11		3	21	3	17	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN54AS880, SN74AS880

DUAL 4-BIT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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recommended operating conditions

			SN54AS880			SN74AS880			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage		2			2			V
V _{IL}	Low-level input voltage		0.8			0.8			V
I _{OH}	High-level output current		−12			−15			mA
I _{OL}	Low-level output current		32			48			mA
t _w	Pulse duration	PRE low	4.5			3.5			ns
		C high	4			2.5			
t _{su}	Setup time, data before C↓		2			2			ns
t _h	Hold time, data after C↓		1			1			ns
T _A	Operating free-air temperature		−55 125			0 70			°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS880			SN74AS880			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	$V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$				–1.2			–1.2	V
V_{OH}	$V_{CC} = 4.5\text{ V to } 5.5\text{ V}$, $I_{OH} = -2\text{ mA}$		$V_{CC}-2$			$V_{CC}-2$			V
	$V_{CC} = 4.5\text{ V}$, $I_{OH} = -12\text{ mA}$		2.4	3.2					
	$V_{CC} = 4.5\text{ V}$, $I_{OH} = -15\text{ mA}$					2.4	3.3		
V_{OL}	$V_{CC} = 4.5\text{ V}$, $I_{OL} = 32\text{ mA}$			0.30	0.5				V
	$V_{CC} = 4.5\text{ V}$, $I_{OL} = 48\text{ mA}$						0.35	0.5	
I_{OZH}	$V_{CC} = 5.5\text{ V}$, $V_O = 2.7\text{ V}$				50			50	μA
I_{OZL}	$V_{CC} = 5.5\text{ V}$, $V_O = 0.4\text{ V}$				–50			–50	μA
I_I	$V_{CC} = 5.5\text{ V}$, $V_I = 7\text{ V}$				0.1			0.1	mA
I_{IH}	$V_{CC} = 5.5\text{ V}$, $V_I = 2.7\text{ V}$				20			20	μA
I_{IL}	$V_{CC} = 5.5\text{ V}$, $V_I = 0.4\text{ V}$				–0.5			–0.5	mA
$I_{O\ddagger}$	$V_{CC} = 5.5\text{ V}$, $V_O = 2.25\text{ V}$		–30		–112	–30		–112	mA
I_{CC}	$V_{CC} = 5.5\text{ V}$	Outputs high		73	118		73	118	mA
		Outputs low		76	122		76	122	
		Outputs disabled		86	137		86	137	

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

SN54AS880, SN74AS880

DUAL 4-BIT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R ₁ = 500 Ω R ₂ = 500 Ω T _A = MIN to MAX				UNIT
			SN54AS880		SN74AS880		
			MIN	MAX	MIN	MAX	
t _{PLH}	D	\overline{Q}	4	11	4	9.5	ns
t _{PHL}			4	9	4	8.5	
t _{PLH}	C	\overline{Q}	6	14	6	11.5	ns
t _{PHL}			4	10	4	8	
t _{PHL}	PRE	\overline{Q}	4	11.5	4	10	ns
t _{PZH}	\overline{OC}	\overline{Q}	2	8	2	7.5	ns
t _{PZL}			4	11	4	10	
t _{PHZ}	\overline{OC}	\overline{Q}	2	8	2	6.5	ns
t _{PLZ}			2	9	2	8	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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