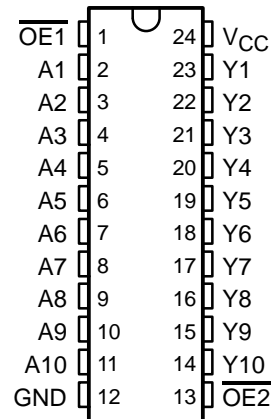


SN74ALS29827, SN74ALS29828 10-BIT BUFFERS AND BUS DRIVERS WITH 3-STATE OUTPUTS

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- Functionally Equivalent to AMD's AM29827 and AM29828
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- pnp Inputs Reduce dc Loading
- Data Flow-Through Pinout (All Inputs on Opposite Side From Outputs)
- Power-Up High-Impedance State
- Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic (NT) 300-mil DIPs

DW OR NT PACKAGE
(TOP VIEW)



description

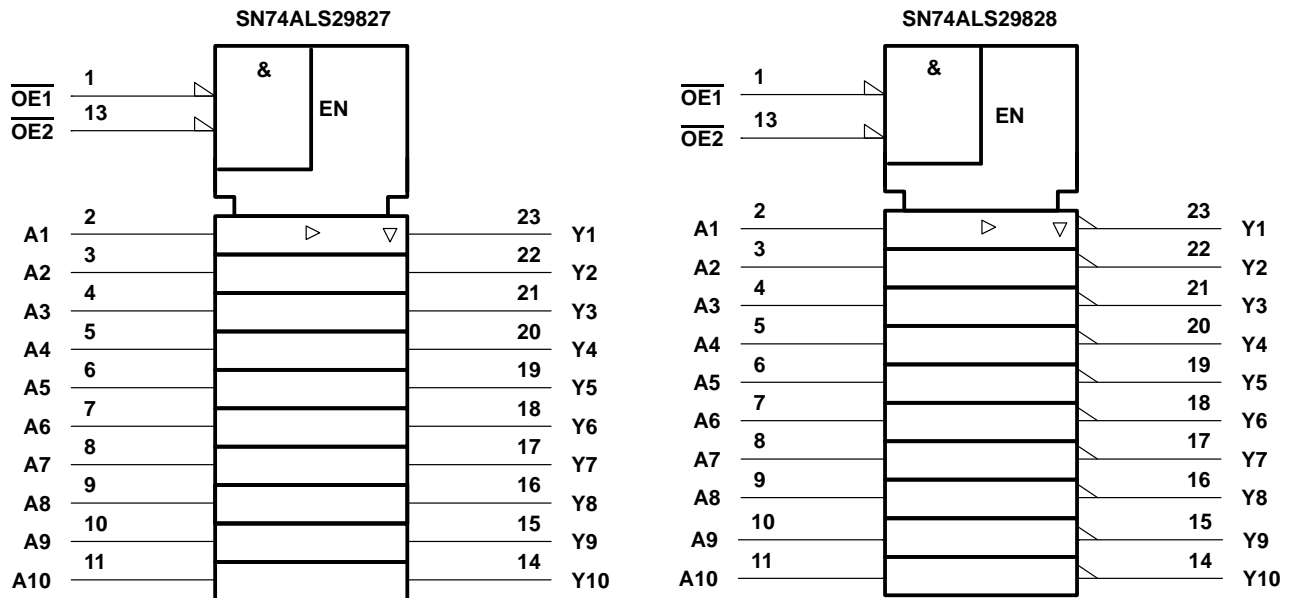
These 10-bit buffers and bus drivers provide high-performance bus interface for wide data paths or buses carrying parity.

The 3-state control gate is a 2-input NOR such that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all ten outputs are in the high-impedance state.

The SN74ALS29827 provides true data and the SN74ALS29828 provides inverted data at their respective outputs.

The SN74ALS29827 and SN74ALS29828 are characterized for operation from 0°C to 70°C.

logic symbols†

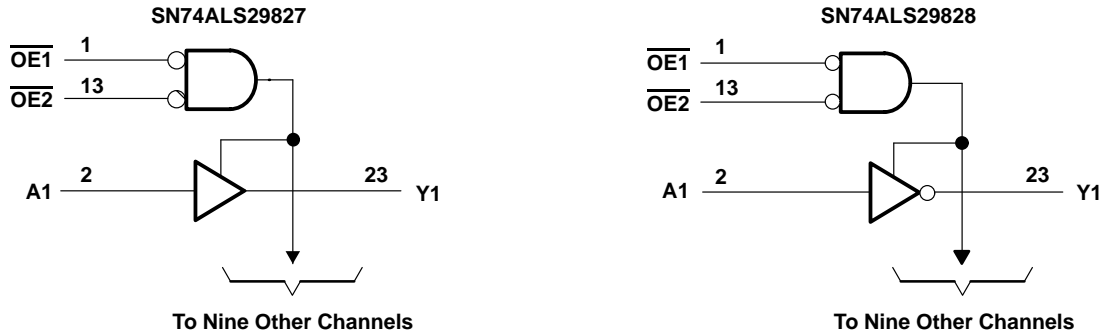


† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN74ALS29827, SN74ALS29828 10-BIT BUFFERS AND BUS DRIVERS WITH 3-STATE OUTPUTS

SDAS095B – JANUARY 1986 – REVISED JANUARY 1995

logic diagrams (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC}	7 V
Input voltage, V_I	5.5 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN74ALS29827 SN74ALS29828			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			–24	mA
I_{OL}	Low-level output current			48	mA
T_A	Operating free-air temperature	0		70	°C

SN74ALS29827, SN74ALS29828
10-BIT BUFFERS AND BUS DRIVERS
WITH 3-STATE OUTPUTS

SDAS095B – JANUARY 1986 – REVISED JANUARY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN74ALS29827 SN74ALS29828		UNIT
			MIN	TYP†	
V _{IK}	V _{CC} = 4.75 V,	I _I = −18 mA	−1.2		V
V _{OH}	V _{CC} = 4.75 V	I _{OH} = −15 mA	2.4		V
		I _{OH} = −24 mA	2		
V _{OL}	V _{CC} = 4.75 V,	I _{OL} = 48 mA	0.35	0.5	V
I _{OZH}	V _{CC} = 5.25 V,	V _O = 2.4 V	20		μA
I _{OZL}	V _{CC} = 5.25 V,	V _O = 0.4 V	−20		μA
I _I	V _{CC} = 5.25 V,	V _I = 5.5 V	0.1		mA
I _{IH}	V _{CC} = 5.25 V,	V _I = 2.7 V	20		μA
I _{IL}	V _{CC} = 5.25 V,	V _I = 0.4 V	−0.1		mA
I _{OS} ‡	V _{CC} = 5.25 V,	V _O = 0	−75	−250	mA
I _{CC}	V _{CC} = 5.25 V		25	40	mA

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V _{CC} = 4.75 V to 5.25 V				UNIT
				SN74ALS29827		SN74ALS29828		
				MIN	MAX	MIN	MAX	
t _{PLH}	A	Y	C _L = 300 pF	15	14	ns		
t _{PHL}				15	14			
t _{PLH}	A	Y	C _L = 50 pF	8	7	ns		
t _{PHL}				8	7.5			
t _{PZH}	\overline{OE}	Y	C _L = 300 pF	20	20	ns		
t _{PZL}				23	23			
t _{PZH}	\overline{OE}	Y	C _L = 50 pF	15	15	ns		
t _{PZL}				15	15			
t _{PHZ}	\overline{OE}	Y	C _L = 50 pF	17	17	ns		
t _{PLZ}				12	12			
t _{PHZ}	\overline{OE}	Y	C _L = 5 pF	9	9	ns		
t _{PLZ}				9	9			

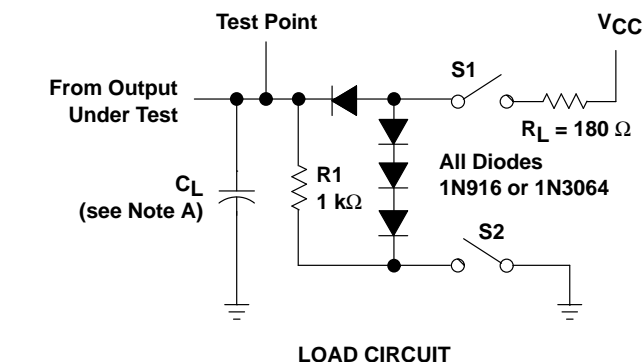
SN74ALS29827, SN74ALS29828

10-BIT BUFFERS AND BUS DRIVERS

WITH 3-STATE OUTPUTS

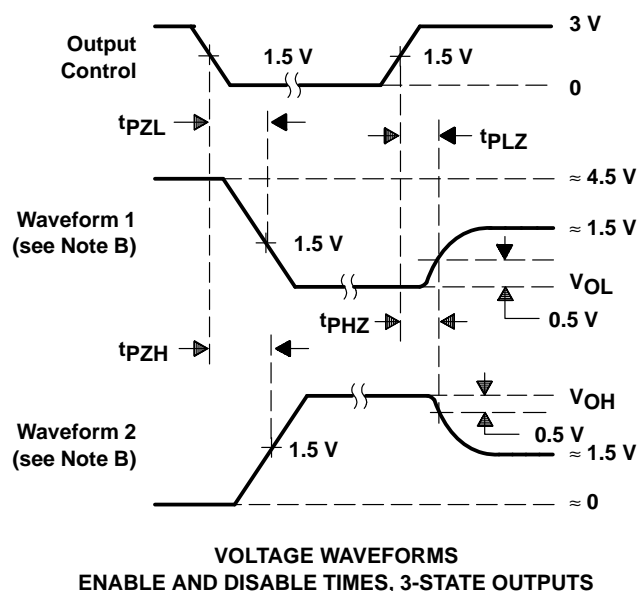
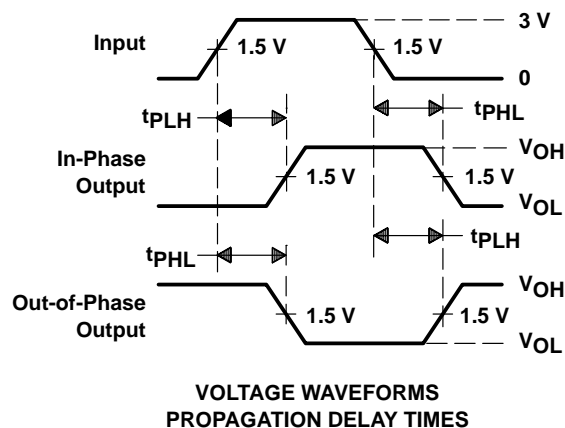
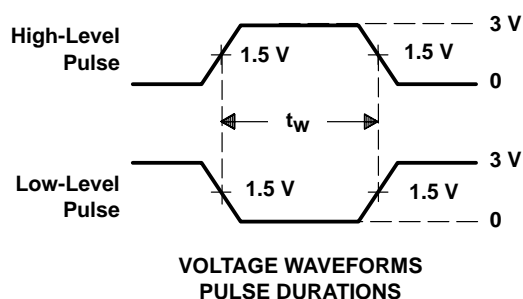
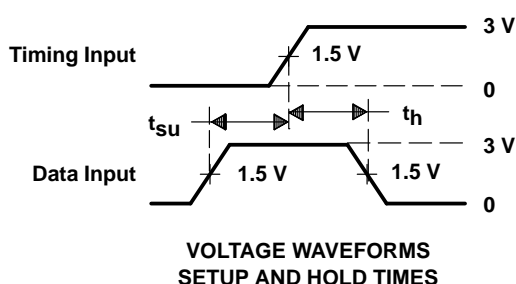
SDAS095B – JANUARY 1986 – REVISED JANUARY 1995

PARAMETER MEASUREMENT INFORMATION



SWITCH POSITION TABLE

TEST	S1	S2
t_{PLH}	Closed	Closed
t_{PHL}	Closed	Closed
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed



- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.

Figure 1. Load Circuit and Voltage Waveforms

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